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"Mas não basta pra ser livre
Ser forte, aguerrido e bravo
Povo que não tem virtude
Acaba por ser escravo"

(Hino Rio-Grandense)

ZnO Thin-Film Transistors for Cost-Efficient Flexible Electronics

by Fábio Fedrizzi Vidor

Flexible and transparent electronics enable the integration of innovative cost-efficient products. One of the outstanding aspects of this technology is its wide range of applications; from flexible and transparent displays to wearable electronics and RFID (radio-frequency identification) tags for sensor networks employed, for instance, in health monitoring systems. In this area, thin-film transistors (TFTs) are the key elements which drive the electrical currents in the devices. Conjointly, hybrid systems, combining high performance silicon-based transistors for data processing and thin-film transistors for enhanced user interactivity, emerge profiting from the synergy of both technologies.

In this study, ZnO-based TFTs for flexible and transparent electronics were integrated and characterized. The fabrication processes were limited to cost-efficient and low-temperature methods compatible to large area flexible substrates; therefore, solution-based techniques were primary applied. For the active semiconductor, ZnO precursors and dispersions containing nanostructures of the material were evaluated; the latter depicting better compatibility with the integration process as well as higher performance and reliability. As gate dielectric, poly(4-vinylphenol) (PVP) and a high-k nanocomposite were employed. The transistors were structured in both inverted staggered and inverted coplanar setups. On the one hand, the staggered structures depict larger contact area between the drain/source electrodes and the active semiconducting layer, hence higher charge carrier injection. On the other hand, their coplanar counterparts profit from the late semiconductor deposition, which enables an effective analysis of the instabilities concerning the transistor. To investigate the performance metrics and reliability issues, an extensive characterization of the transistors was performed. After the main instability effects were identified and mitigated, the TFTs were also integrated on polymeric substrates. Aiming at the fabrication of compact and energy-efficient devices, optical photolithography was used for layer patterning instead of shadow mask technique. Along with the resolution of around 1 μm achieved for multiple layer definition, the employment of freestanding PET substrates reproduces a more realistic scenario for a later large-scale production. Different methods, namely spin- and spray-coating and doctor blade technique, for the semiconductor dispersion deposition were investigated, leading only to minor variations on the TFT electrical performance. The metrics of the integrated ZnO nanoparticle TFTs are among the best reported for nanoparticle-based transistors up to date. Additionally, they are comparable to those of TFTs fabricated using cost-intensive techniques or high-temperatures processes.

In order to evaluate the ZnO TFTs in electronic circuit applications, inverters employing an active transistor in the pull-down network and a load transistor in the pull-up network were integrated on rigid and on flexible substrates. Furthermore, the dynamic characteristics of such inverters were analyzed in ring oscillator circuits. Finally, by an adaptation of the photolithography, self-alignment processes were used to reduce the transistor's parasitic capacitances as well as to pattern the semiconducting layer in order to avoid cross-talk effect between devices. Furthermore, a complementary design using n-type inorganic and p-type organic TFTs is evaluated.

ZnO Dünnschichttransistoren für eine kostengünstige flexible Elektronik

von Fábio Fedrizzi Vidor

Flexible und transparente elektronische Schaltungen ermöglichen eine Integration von innovativen und kostengünstigen Produkten in einem breiten Anwendungsspektrum, z. B. von flexiblen und transparenten Displays für tragbare Elektronikprodukte bis hin zu RFID Funketiketten, entwickelt für Sensornetzwerke im Bereich des Gesundheitssektors. Hierbei sind Dünnschichttransistoren (TFTs) die Schlüsselelemente zur Steuerung des Stromflusses in den Bauelementen. Ferner erscheinen hybride Systeme, zum einen aus hochfrequenten Siliziumtransistoren für die Datenverarbeitung, zum anderen aus Dünnschichttransistoren zur Erhöhung der Interaktivität mit dem Nutzer, profitabel, da sie in Synergie die Vorteile beider Technologiezweige vereinen.

Während dieser Arbeit wurden TFTs auf ZnO-Basis für die flexible und transparente Elektronik integriert und charakterisiert. Der Herstellungsprozess war auf kostengünstige Methoden, die eine Kompatibilität mit großflächigen flexiblen Substraten aufweisen, beschränkt. Aus diesem Grund wurden hauptsächlich lösungsmittelbasierende Verfahren verwendet. Für den aktiven Halbleiter wurden Präkursoren und Dispersionen, die ZnO-Nanostrukturen enthalten, bewertet. Hierbei zeigten die Dispersionen neben ihrer besseren Kompatibilität mit den Integrationsprozessen eine höhere Leistungsfähigkeit und Beständigkeit. Als Gate-Dielektrikum wurden Poly(4-vinylphenol) sowie ein high-k Nanokompositlack eingesetzt. Die TFTs wurden sowohl im inverted staggered als auch im inverted coplanar Aufbau strukturiert. Einerseits weisen die inverted staggered Strukturen eine größere Kontaktfläche zwischen den Drain/Source Elektroden und der aktiven Halbeiterschicht und damit eine verbesserte Ladungsträgerinjektion auf. Andererseits profitiert die coplanare Bauform von der späten Halbleiterdeposition, welche eine effektive Analyse der Instabilitäten während des Transistorbetriebs ermöglicht. Nachdem die Hauptursachen für Instabilitäten während des TFT-Betriebs identifiziert und reduziert wurden, erfolgte die Integration auf polymeren Substraten. Um die Herstellung von kompakten und energieeffizienten Bauelementen zu ermöglichen, wurde die optische Fotolithographie mit einer maximalen Auflösung von 1 μm verwendet. Ferner zeigte der Einsatz von freistehenden PET Substraten ein realistischeres Szenario für eine spätere, reproduzierbare Herstellung von großflächigen Produkten. Obwohl verschiedene Halbleiterdepositionsmethoden untersucht wurden, zeigte sich nur eine geringfügige Variation in den Charakteristiken der TFTs. Die elektrischen Charakteristika der in dieser Arbeit integrierten ZnO-Nanopartikel TFTs gehören gegenwärtig zu den Besten der auf Nanopartikel basierenden TFTs und sind sogar mit der Leistungsfähigkeit von Dünnschichttransistoren vergleichbar, die mit kostenintensiven Techniken oder Hochtemperaturprozessen hergestellt wurden.

Um mögliche Anwendungsgebiete für ZnO TFT Schaltungen zu untersuchen, wurden Inverterschaltungen und Ringoszillatoren auf starren und flexiblen Substraten hergestellt und analysiert. Durch die Anpassung der verwendeten fotolithographischen Prozessschritte wurde zum einen die Selbstjustierung der Drain/Source Elektroden zur Reduzierung der parasitären Transistorkapazitäten erreicht. Zum anderen konnte hierdurch die integrierte Halbleiterschicht strukturiert werden, um Crosstalk-Effekte zwischen den einzelnen Bauelementen zu vermeiden. Weiterhin wurde ein komplementäres Design unter Verwendung von anorganischen n-Kanal und organischen p-Kanal TFTs evaluiert.

Transistores de filmes finos de ZnO para a eletrônica flexível e de custo eficiente

de Fábio Fedrizzi Vidor

A eletrônica flexível e transparente proporciona a fabricação de produtos inovadores e de boa relação custo-benefício. Uma das vantagens desta tecnologia é sua ampla área de aplicações; desde telas flexíveis e transparentes até eletrônica vestível e etiquetas RFID (identificação por radiofrequência) usadas em rede de sensores, por exemplo, para monitoração de saúde. Nestas áreas, transistores de filmes finos (TFTs) são os elementos essenciais para a condução de corrente elétrica no dispositivo. Além disso, sistemas híbridos, que combinam transistores de silício para o processamento de dados e TFTs para a melhoria da interatividade do usuário, emergem beneficiando-se da sinergia de ambas as tecnologias.

Neste estudo, TFTs utilizando ZnO são integrados e caracterizados visando a eletrônica flexível e transparente. Os processos de fabricação foram limitados a métodos de baixo custo e compatíveis a substratos flexíveis com grandes superfícies; portanto, técnicas que utilizam soluções foram preferencialmente aplicadas. Para o semicondutor ativo, precursores de ZnO e dispersões contendo nanoestruturas deste material foram avaliados; sendo que a última variação apresentou melhor compatibilidade com os processos de integração assim como melhor performance e confiabilidade. Como dielétrico de porta polivinilfenol (PVP) ou um nanocomposto de alta performance foi usado. Os transistores foram estruturados nas configurações *inverted staggered* e *inverted coplanar*. Enquanto a estrutura *staggered* apresenta maior área de contato entre o semicondutor e os contatos de dreno e fonte, logo uma maior injeção de portadores; a estrutura *coplanar* tem a vantagem da tardia deposição do semicondutor, o que permite uma melhor avaliação dos efeitos de instabilidades. Para uma melhor avaliação dos transistores, uma extensiva caracterização elétrica foi conduzida. Após os fatores críticos responsáveis pela instabilidade dos TFTs serem identificados e mitigados, os dispositivos foram integrados em substratos flexíveis. Visando a integração de dispositivos compactos, litografia óptica foi utilizada para a estruturação dos filmes ao invés de *shadow masks*. Além da resolução de cerca de $1\,\mu$m alcançada, o uso de substrato sem fixação reproduz um cenário mais realístico para produção em massa. Também, diferentes métodos para a deposição do semicondutor foram avaliados, resultando em variações mínimas nas características elétricas dos TFTs. Além disso, estas características estão entre as melhores reportadas para TFTs com nanopartículas de ZnO até o momento. Elas também são comparáveis às de transistores produzidos com técnicas de alto custo e altas temperaturas.

Visando a aplicação dos transistores em circuitos eletrônicos, inversores utilizando um transistor de controle na rede de *pull-down* e um transistor de carga na rede de *pull-up* foram integrados em substratos rígidos e em flexíveis. Osciladores em anel também foram fabricados para a caracterização dinâmica dos dispositivos. Além disso, uma adaptação no processo fotolitográfico (auto-alinhamento) foi demostrada a fim de reduzir capacitâncias parasitas e estruturar o filme semicondutor (para reduzir efeito de *cross-talk*). Por fim, um design complementar utilizando transistores inorgânicos (tipo N) e orgânicos (tipo P) foi avaliado.

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This dissertation is dedicated to my wife, Jéssica, whose love and support have been a continual inspiration. She is more than my wife, she is my best friend. During our entire stay in Germany, she was always there motivating and pushing me to my best (work and life). Thank you for being this strong woman, thank you for letting your life in Brazil to

establish our live together in a foreign country and to explore by my side a little bit more of the world (by the way, we still have many and many travels ahead us). I love you my darling!

At the end, I would like to express my gratitude to my family:

No dia que me tornei engenheiro eletricista, a música em homenagem aos pais foi "Conselhos" de Wilson Paim. Pois bem, ela não é mais "apenas" uma música que tocou na formatura ou que tocava durante nossas viagem pelo Brasil e pela América Latina:

"Filho, agora é chegada a hora,
de saires campo afora,
rumo a estância do saber
(...)
Anda, vai e doma a leitura,
te amansa em literatura,
e prende no laço a ciência,
que ao longo de tua ausência,
hei de rezar ao senhor,
prá que voltes à querência,
um verdadeiro doutor."
(Conselhos – Wilson Paim)

Pai e mãe, fomos e voltamos! Obrigado de todo o coração por todo o apoio e por serem esse exemplo tão essencial em nossas vidas. Amamos muito vocês! Também agradeço ao meu irmão Giovani, que apesar das nossas diferenças, se preocupa comigo sempre achando que trabalho de mais. Obrigado a toda a minha família por entenderem a nossa ausência e sempre estarem torcendo por nós. Agradeço também a família da Jé, minha família, especialmente meu sogro Plinio e sogra Graselí, que também estiveram presentes durante toda essa jornada. Amo vocês!

CONTENTS

CHAPTER 1

INTRODUCTION

Products and applications using transparent and flexible electronics are widely connected to a futuristic scenario. They were explored by novels, such as the "Shape of Things to Come" from H.G. Wells in 1933, and by films, such as "Barbarella" based on Jean-Claude Forest's comics in 1968. The animation studio Hanna-Barbera also explored some aspects of future daily artifacts through "the Jetsons" cartoons in the 60s and 80s. Some of the recent Hollywood productions, such as Minority Report (2002) and Ironman (2008, 2010 and 2013) also give us insights of future applications for flexible and transparent electronics and how they can be integrated in our lives. These futuristic visions and ideas motivate the scientific community as well as companies to develop and to employ this technology.

Flexible and transparent electronics enable the fabrication of innovative products making use of different aspects of the applied materials and compounds. Some concepts of applications which take advantages of these characteristics are shown in Figure 1.1. The integration of transparent displays, for example, increases the interactivity of the user with the surrounding environment. Moreover, by employing a flexible substrate, integrated sensor networks can be used as wearable electronic skins enabling, for instance, collection and analysis of body functions for sports and medical applications. The food industry can also profit from this technology: cost-efficient radio-frequency identification (RFID) tags can be employed to monitor food quality and storage conditions in real time. For these applications, thin-film transistors (TFTs) are commonly used as active

Figure 1.1: Concept applications of transparent and flexible electronics in the field of displays, sensor networks for medical monitoring and for sport activity, and RFID tags for the food industry.

circuit elements. The advantages of this type of transistors are: the integration process almost independent of the substrate (generally used just as mechanical support), and the opportunity to apply a wide range of materials in its structure. Nevertheless, the TFT technology is not to be seen as a substitute for crystalline silicon (Si) based transistors in the high performance market. This technology should act promoting new products and applications, being implemented in most cases in hybrid systems, to improve data acquisition and user interface.

As this technology avails a wide range of products, the development of new systems itself can be time and cost intensive; one of the main issues is dealing with the feasibility and with the complexity of the whole project. Therefore, the use of abstraction levels leads to a more effective development of the technology. Figure 1.2 shows an example of a schematic design of abstraction levels for transparent and flexible systems. In this particular case, the main focus has been given to its electronic part, nevertheless the same method can be also directed to the mechanical and aesthetic aspects of the product. Each abstraction level can use the previous one as a black box or as a model avoiding unnecessary internal complexity and focusing on the developing of the current level elements. In the example of Figure 1.2, the system was divided into different levels in order of increasing abstraction: materials, devices, circuits, modules, and the system itself. The focus of this study is

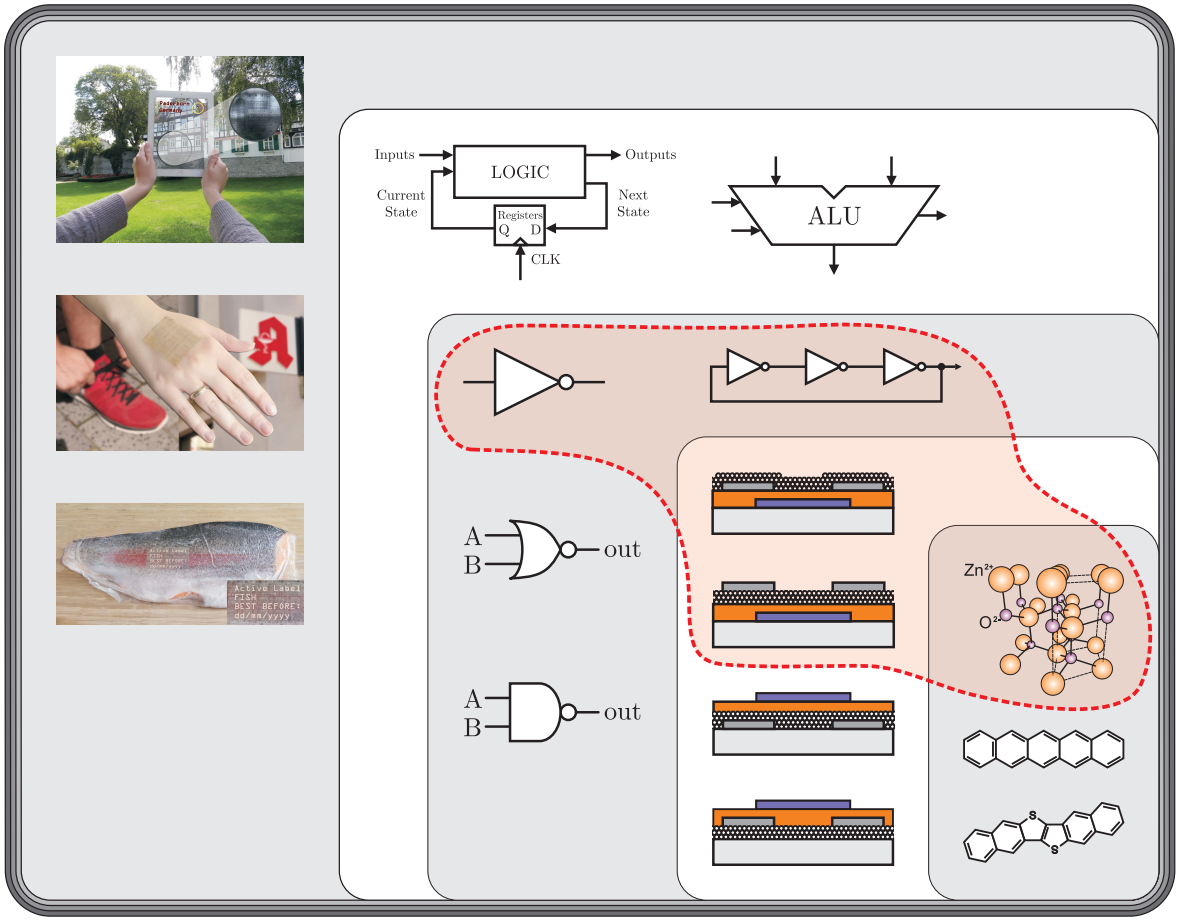


Figure 1.2: Schematic design of abstraction levels for flexible and transparent systems. The selection in red depicts the levels covered in this dissertation.

placed in the device level; however, a merge with both frontiers (materials and circuits) is also covered.

The purpose of this dissertation is the development of cost-efficient inorganic-based thin-film transistors and circuits on flexible and transparent substrates employing low-temperature processes. Aiming at reduced costs, solution-based materials are preferred for the integration of the TFTs. The use of solution-based techniques fulfills the large area integration and flexible substrates requisites, while exhibiting advantages when compared to cost-intensive vacuum-based processes. Among inorganic materials, metal oxides dominate the sector with different compounds and deposition methods, which can be selected depending on the system requirements [WS09, FBM12, PMV+16]. Zinc oxide (ZnO) has emerged as a primary compound in this field, possessing outstanding electrical and chemical characteristics as well as being transparent to the visible light spectrum. Therefore, solution-based processes employing either ZnO precursors or a dispersion containing nanostructures of the material are chosen for the formation of the active semiconducting layer. Besides the investigation of different gate dielectric materials as well as deposition methods for the semiconductor, it is also an objective of this study to identify and minimize the agents responsible for instabilities effects in the transistor operation. Further studies should be conducted to analyze the TFTs characteristics upon different transistor structures on either rigid (oxidized Si or glass wafer) or on polymeric substrates. Moreover, the integration and evaluation of the transistors in digital circuits, *e.g.* inverter circuits and ring oscillators, is also sought.

1.1 Structure of the Work

Initially, the fundamentals concerning thin-film transistors and flexible electronics are presented in Chapter 2. The discussion comprises the intrinsic attributes of the active semiconducting material employed in this study, important aspects related with TFTs, such as its history and a comparison with high performance Si-based transistors, as well as their operation properties, modeling and electrical characterization.

Chapter 3 is devoted to the integration process of the transistors on rigid and on flexible substrates. Therefore, TFT basic structures and each of its components are addressed. Although the focus is given to the processes and methods applied in this study, a general overview of the most used techniques and materials found in the literature is given.

The electrical characterization of the TFTs are mainly presented in Chapter 4. Transistors integrated employing ZnO precursor or nanoparticles as well as a discussion concerning the electron flow mechanism in the nanoparticulated semiconducting film and its effect on the transistor's current are described. Along with the I-V curves, qualitative models representing the TFT behaviors are given and analyzed.

Chapter 5 addresses the performance of circuits integrated employing the ZnO-based TFTs. Whereby, inverter circuits integrated using load-transistors in the pull-up network and active-transistors in the pull-down network on rigid and on flexible substrates are analyzed. Additionally, their dynamic characteristics (ring oscillator circuits) are evaluated.

Improvements for the integrated circuits and devices are presented in Chapter 6. Approaches such as the reduction of parasitic capacitances and of cross-talk effects, implementation of a complementary design applying both *n*-type ZnO-based TFTs and *p*-type organic-based TFTs, and evaluation of further deposition methods for the active semiconducting material are addressed.

Finally, in Chapter 7, the main conclusions of this dissertation as well as future perspectives for ZnO-based TFTs and flexible electronics are discussed.

1.2 Remarks on the Reference Style

Third party authors are represented by [XXXYY], where "XXX" is the author's initials and "YY" is the publication year.

The references I am author or co-author are numbered, *i.e.* [1],[2],..., chronologically and categorized as presented in Section: *Publications*. Therefore, when these references are cited in this dissertation, they will not follow an ascending numeration. This method was chosen to state in a clear way to which of the references the author of this dissertation has contributed.

CHAPTER 2

FUNDAMENTALS

Since its conception at the Bell Laboratories in 1947, the transistor has become one of the most important cornerstones of technology development. Currently, transistors are employed in a wide array of applications, such as computers, telecommunications, data storage and sensor networks. For the future, the mass connectivity predicted by the Internet of Things (IoT) and the Internet of Everything (IoE) has placed the transistor in a pivotal role of scientific and economic development. Therefore, Si-based devices are expected to be found in almost every application in nearly any field. The use of Si as the primary active semiconducting material in microelectronics was mainly driven by a high quality and stable oxide - silicon dioxide (SiO_2). In the 60s, Gordon Moore projected that the semiconductor industry would double the number of components on a chip every two years [Moo65], which has led the industry to constantly push further the technology boundaries to maintain the trend. Therefore, even though the core of the silicon metal-oxide-semiconductor field-effect transistor (MOSFET) has remained the same over the years, several technological adaptations on its structures have been made. Innovative approaches, on device level and on circuit design level, were used to solve the non-idealities issues inherent from the current small dimensions of the devices. At first, the main focus was to improve the device performance. Nowadays, two main trends are observed for silicon-based devices, one focused on the performance (*e.g.* servers) and the other on low-power consumption (*e.g.* portable applications).

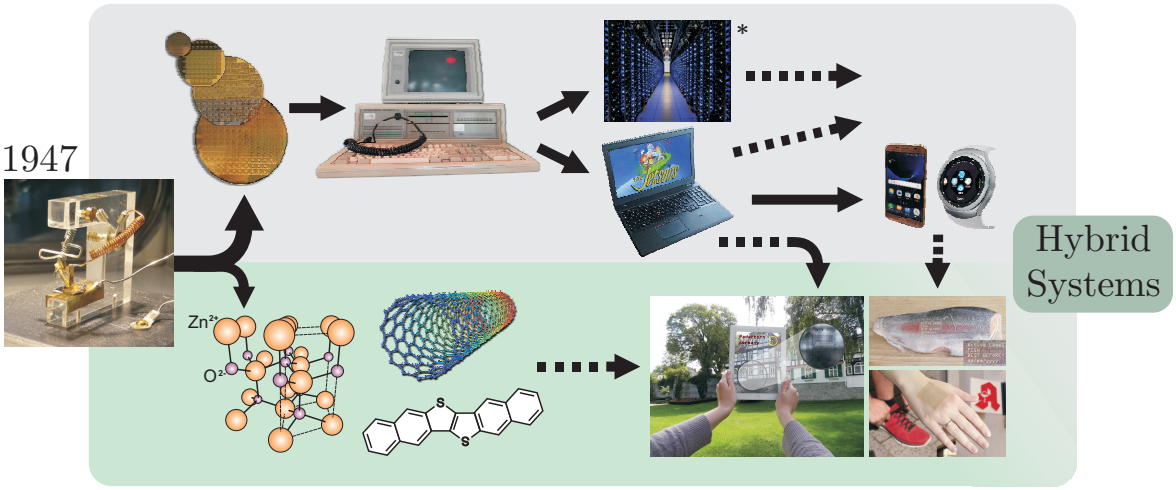


Figure 2.1: Evolution of the transistor technology and its applications. (* Image from Google Inc.)

Besides the improvements in the microelectronic technology to avail the integration of billions of transistors in a single chip with effective computational power, there are other applications that do not necessarily require high performance and high device density. The possibility to fabricate devices on large area substrates using low-temperature processes and exploring the materials characteristics in a wider range expands the device application fields. This approach benefits applications such as chemical and biological sensor networks, active matrix elements for pixel driving in displays, RFID tags, wearable and flexible electronics, for instance. For these purposes, thin-film transistors are the key elements for the driving currents in the system. They are less cost intensive than MOSFETs, and they are used in applications where high performance is not the main requirement, as shown in Figure 2.1. Moreover, this sort of transistors is not planned to be a substitute for the crystalline-Si-based transistors in the high performance market. The main goal of this technology is to add new functionality to already existing and newly created products and applications, giving rise to hybrid systems. In this way, the main data management is done by high performance transistors, whereas the data acquisition and the user interaction features are accomplished by flexible and transparent TFTs.

Regarding the density of integrated devices per unit area, another difference between the TFT and MOSFET markets is observed. Figure 2.2a depicts the evolution over the years for both technologies. While high performance MOSFETs are still following Moore's law with the number of transistors doubling every couple of years; the TFT technology has mainly focused on stability, reproducibility and cost reduction of fabrication processes,

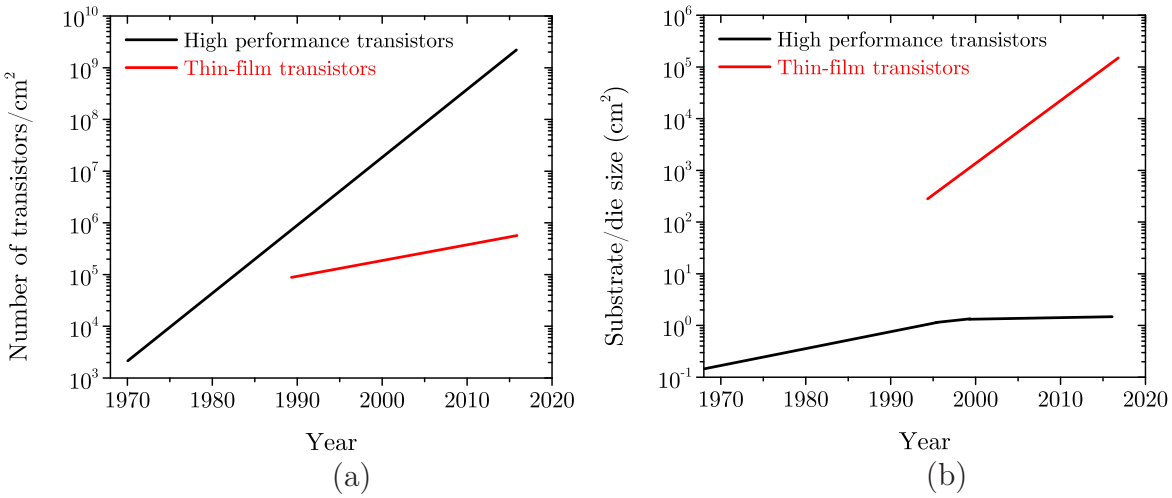


Figure 2.2: Comparison between the MOSFET and TFT technologies concerning (a) the number of transistor per unit area and (b) the substrate/die size over the years. Plots are approximations of Moore's Law, and of current data from MOSFETs [Hru14] and TFTs (based in the display market) [Str09]. Adapted from [Fra15].

which are independent of the substrate size. The scenario associated to the substrate/die size is the opposite. Even with the significant increase of the wafer size (diameter of around 300 mm) in modern MOSFET production, the die size for a single chip has not notably increased in order to maximize the yield and reduce the costs. Conversely, the integration of TFTs benefits from the development of processes suitable to large area substrates; thus, a rapid increase of the substrate size along the years is observed (Figure 2.2b).

The basic concepts of TFT integration and operation are not new. The first patent regarding its functionality dates from 1933 [Lil33], years before the presentation of a operating device by Weimer in 1961-1962 [Wei61, Wei62]. He described a TFT using polycrystalline cadmium sulfide (CdS) as the active semiconductor, gold (Au) for the metal contacts and silicon monoxide (SiO) as the gate dielectric. Conjointly, vacuum techniques were used in the integration process as well as shadow masks for the structuration of the layers. Around the same time, transparent metal oxide TFTs were also investigated, as for example, the SnO_2-based TFTs on a glass substrate presented by Klasens and Koelmans [KK64]. They were integrated employing aluminum (Al) for the metal contacts and aluminum oxide (Al_2O_3) as gate dielectric; however, the main focus was given to a self-aligned procedure for the drain and source electrodes, and not to the materials themselves. ZnO-based TFTs were first reported by Boesoen and Jacobs in 1968 [BJ68]. Nevertheless, these TFTs showed inferior performance in comparison with the emergent MOSFETs [HH63] which depicted remarkable electrical properties suitable

for integration in high performance systems. Despite MOSFETs being the focal point of the technology, TFTs have found a market niche: the control of each pixel in liquid crystal displays (LCDs), as proposed by Lechner *et al.* in 1971 [LMNT71]. Just in 1979 with the introduction of hydrogenate amorphous silicon (a-Si:H) as active semiconductor material, the TFTs have become interesting as switching element in LCDs maintaining low production costs, good reproducibility and uniformity on large area substrates, as well as adequate electrical characteristics. Their performance was improved by the employment of polycrystalline silicon (poly-Si) as active semiconductor [KA03]. However, in this case, high-temperature processes are required unavailing the integration on soda-lime glass. Another approach is the use of a low-temperature process for the deposition of poly-Si, which drastically increases the production costs [LKT+91, LTK+91].

The introduction of organic semiconducting materials in the 90s has also impacted the TFT technology [Sir14]. Organic-based TFTs presented electrical characteristic comparable to a-Si:H-based transistors [GHPF90], despite using low processing temperatures. Organic compounds were considered as one of the future materials for TFTs integration and thus the future of flexible electronics. Different kinds of thiophene derivates and pentacene were analyzed evaluating their performance for TFT technology [Sir14]. Even presenting good electrical characteristics, degradation effects due to humidity and oxidation in ambient atmosphere limited the life-time of such systems and prevented a straight forward employment of these compounds [Sir14, PDH04]. As a solution, passivation layers or encapsulation were required to avoid these effects, increasing production costs. On the other hand, new synthesized thiophene derivates, such as DNTT and C_8-BTBT, have shown better electrical stability to ambient air due to their larger ionization potentials. Therefore, they are currently researched by different groups and institutions [ZAK+11, Sir14, LML+11]. While *p*-type organic-based TFTs performance has improved significantly over the years, *n*-type transistors are still under research and struggling to achieve comparable electrical characteristics [Sir14].

In this scenario, another group of inorganic compounds has reemerged as a solution for the integration of *n*-type TFTs at low cost and for transparent electronics: the metal-oxide compounds. Aside from the first trials using them as active semiconductor in TFTs in the 60s, metal-oxide-based TFTs have attracted worldwide attention with the reports from Hoffman *et al.* [HNW03], Masuda *et al.* [MKO+03] and Carcia *et al.* [CMRN03] in 2002-2003. The main aspects reported in these works are: (I) the similar or even better performance in comparison to a-Si:H-based and to organic-based TFTs , (II) the feasibility to

integrate fully transparent TFTs using just oxides-based materials [HNW03, MKO+03], and (III) the deposition of the layers at room temperature using radio-frequency (RF) sputtering technique [CMRN03]. After these publications, the number of scientific groups researching metal oxides increased significantly aiming towards performance improvement, without employing high-temperature processes or increasing the costs of the fabrication. TFTs based on binary compounds such as ZnO, In_2O_3 and SnO_2 were primary studied. However, with the introduction of complex compounds as InGaZnO (GIZO) by Nomura *et al.* [NOU+03], other oxide compounds such as ZnSnO (ZTO), InZnO (IZO), InGaO (IGO) and GaZnO (GZO) were also investigated as possible active semiconductors [HMW09, PYBL08, ETT+12, VKJ+08]. Aiming at a higher performance, vacuum processes, such as sputtering technique and atomic layer deposition (ALD), were used enabling denser films at low temperatures [FPP+04, LKKP07, PHJ+08]. Nevertheless, such films have still high production costs due to the required vacuum systems. Moreover, when large area substrates are used, the equipment size restrains the maximum size. In order to reduce production costs and to enable the integration on larger substrates, solution-based techniques have gained significant attention, providing cost-efficient devices. One of the main advantages of employing solution-based materials (nanoparticles dispersion and precursors) is the variety of possible deposition methods. Spin-coating is still the most used and reported one by the scientific community [KYK14, DJS+15]; although alternative techniques, like inkjet printing, spray-coating, doctor blade, gravure imprinting and Meyers rods, allow the integration of low-cost devices on large area and flexible substrates either using organic or inorganic compounds and, therefore, are actively researched [YGA+14, DTG+13, MAH+08, MSR+14, PMV+16, YPPK14].

The Paderborn University has also contributed to the TFT technology development for both organic- and inorganic-based transistors. A review of the work aiming at the integration of flexible electronic systems done at the Sensor Technology Department can be found in [6]. Starting with pentacene-based TFTs, degradation effects on organic compounds as well as the evaluation of dielectric layers were studied. Switching to inorganic semiconducting materials, the focus was given to Si-nanoparticle-based TFTs. On account of the oxide shell observed on the Si nanoparticles, the transistor performance is limited. For this reason, metal oxide nanoparticles as ZnO, in which an insulating shell is absent, were evaluated and showed better electrical characteristics [33]. In line with previous researches from the group, the main topic of this dissertation is the integration and characterization of ZnO-based TFTs using flexible substrates for the low-cost sector.

Prior to the analysis and discussion of the TFTs, a review of the main characteristics related to the active semiconductor (ZnO) and to the TFT functionality is presented.

2.1 ZnO Properties

As discussed previously, inorganic materials, in particular metal-oxide compounds, exhibit inherent properties to be employed in low-cost applications. Among them, ZnO-based materials have shown promising characteristics, not only based on their electrical properties but also due to their chemical, sensorial and optical ones [JP06]. Even though the growing interest in ZnO for its semiconducting characteristics is recent, the compound itself has been used in other areas for over a century. The employment of ZnO in cosmetics and in health care products as facial powders, ointments and sunscreens as well as in catalysts, lubricants additives, paint pigmentation, piezoelectric transducers, varistors and transparent conducting electrodes shows the wide range of applications and the versatility of this compound. The main applications concerning its semiconducting properties are related to blue/UV optoelectronics and to its employment as active semiconductor material for the integration of transparent and flexible transistors and solar cells.

ZnO belongs to the group-II-VI binary compound semiconductors and it crystallizes in wurtzite, zinc blend and rocksalt structures [ÖAL+05, Kli07]. At ambient conditions, the thermodynamically stable phase is the wurtzite crystal structure, shown schematically in Figure 2.3. This hexagonal lattice is characterized by two interconnecting sublattices of Zn^{2+} and O^{2-}, such that each cation is surrounded by four anions at the corners of a tetrahedron and vice versa [ÖAL+05, Kli07]. This atom arrangement is typical of sp^3 covalent bonding; nevertheless, it also depicts a substantial ionic character. Therefore, ZnO is a semiconducting material, whose ionicity resides on the borderline between covalent and ionic semiconductor. Additionally, ZnO is a direct semiconducting material as the global extrema of the uppermost valence and lowest conduction bands are aligned at the Γ-point at the Brillouin zone. The band gap is about 3.44 eV at 4.2 K [Kli07]. The minimum of the conduction band is formed by the empty 4 s states of the Zn^{2+} or the antibonding sp^3 hybrid states. The maximum of the valence band is originated from the occupied 2 p orbitals of the O^{2-} or from the bonding sp^3 orbitals [MAH+04, Kli07]. The ZnO uppermost part of valence band is split into three states (A, B and C) by spin-orbit and crystal-field splitting [MAH+04, Kli07]. The ZnO fundamental band gap diagram at

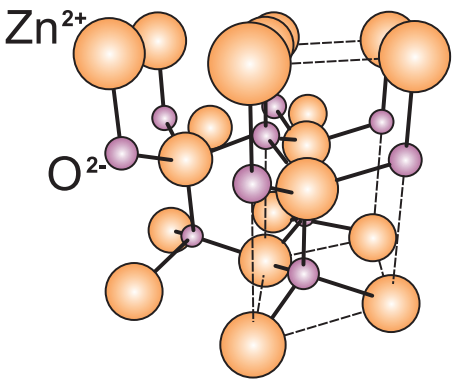


Figure 2.3: ZnO's wurtzite crystal structure. One unit cell is outlined (dashed line) for clarity. Adapted from [JP06].

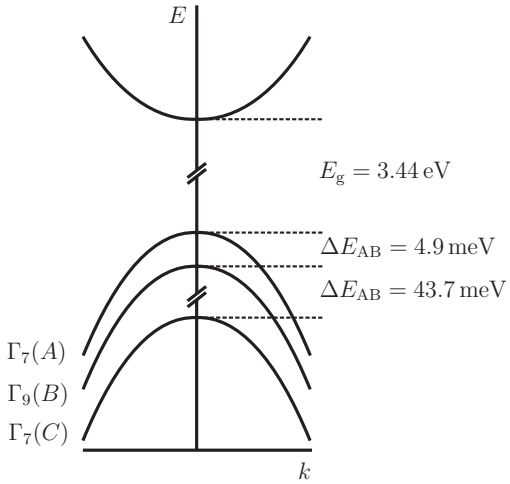


Figure 2.4: Schematic band gap of ZnO at the Γ-point considering the crystal-field and spin-orbit splitting of the valence band at 4.2 K. Adapted from [MAH+04, Kli07].

low temperature (4.2 K) is shown in Figure 2.4. At room temperature (300 K) the band gap is about 3.3 eV [MAH+04].

Despite the prediction that ZnO is an intrinsic semiconductor, it is predominantly found as *n*-type semiconducting material. The nature of the residual *n*-type conductivity is attributed either to the presence of a high concentration of native defects in the form of oxygen vacancies (V_o) and zinc interstitials (Zn_i), or to hydrogen, which occurs exclusively in the positive state in ZnO; *i.e.* it always acts as a donor [JP06, JV05, JV07]. The exact origin for the *n*-type conductivity without an aimed doping is still under debate and not entirely understood [JP06, JV07, ÖAL+05, Kli07]. For the *n*-type doping of ZnO, elements from the group-III as Al, Ga, and In substitute the Zn, or elements from the group-VII as Cl and I substitute O from the ZnO crystal structure acting as donor

dopants [KSMY02]. The n-doping of ZnO has already been investigated by several groups; as a result, high quality and low impedance n-type ZnO films are achievable [ABD$^+$95, MBL$^+$97, KCH$^+$00, LSL$^+$03]. On the other hand, the obtaining of reproducible and reliable p-type ZnO is quite difficult, because of the carrier compensation by native defects of ZnO [Wal94, PZW02, LJS$^+$03, FBM12, PMV$^+$16].

The interaction of metal-oxide compounds with the ambient air has been focus of research of different scientific groups [Con10, Rot04, MSF$^+$13, JP06, CZ92]. Zinc oxide is also influenced by this interaction, hence it is also applied as gas sensor [Mor81, Hir85, XPST00, FL05]. Water and oxygen molecules have a significant impact in the conductivity of ZnO films [Hir85, JWS$^+$08, Wan04] as they are reported to be chemisorbed or physisorbed affecting the charge carrier concentration and distribution in the semiconducting film [Mor81, LDS$^+$09]. The effect of water and of oxygen molecules as well as the influence of UV-irradiation on ZnO and on nanoparticulated ZnO films (used for the TFT integration) are discussed in Section 4.2.

There are different methods to achieve high quality ZnO, which depend on the restrains and requisites of the intended application. Most of the high quality materials are targeted for acoustical and optical devices as a crystalline growth is sought. Methods as RF magnetron sputtering, molecular-beam epitaxy (MBE), pulsed-laser deposition (PLD), metal-organic chemical-vapor deposition (MOCVD) and hydride or halide vapor-phase epitaxy (HVPE) allow a fine control of single crystalline ZnO growth [ÖAL$^+$05, Kli07]. With the improvement of the ZnO growth technology, it is feasible to fabricate ZnO nanostructures. They are available in several forms: nanobelt, aligned nanowire arrays, nanotubes, array of propellers, mesoporous, nanowires, cage and shell structures, nanosprings and spheres [FL05, Wan04, JP06]. Each of these configurations shows distinct properties, which enhance or reduce the effects of specific surfaces of the ZnO crystalline structure [FL05, Wan04, JP06, NQW$^+$08]. For instance, nanowires commonly possess a high length-to-width aspect ratio highlighting specific surfaces. This outcome, together with the form of the nanostructure itself, influences the usability and the performance of each structure according to the application field.

Considering the electrical characteristics, the large direct band gap of the ZnO has some interesting properties as, for instance, high breakdown voltages, ability to sustain large electric fields, low noise generation and high temperature operation [ÖAL$^+$05, Kli07]. Conjointly, ZnO is predicted to be insensitive to the visible light spectrum; therefore,

when the material operates under light exposure, no protective covering is required to avoid light induced instabilities, reducing production costs when compared to light sensitive materials. The electron transport in ZnO materials can be divided in: electron transport at (I) low electric field and at (II) high electric field. When the thermal energy of electrons is higher than the energy gained from the applied field, the energy distribution of the electrons is unaffected by the electric field. Therefore, the mobility is mainly determined by scattering mechanisms and it is independent of the applied electric field, hence the Ohm's law is valid [ÖAL+05]. The major scattering mechanisms that govern ZnO materials are related to Coulomb scattering from ionized impurities or defects, polar optical phonon and piezoelectric scattering, and acoustic-phonon scattering through deformation potentials [ÖAL+05]. In the case when the energy gained by the external field is no longer negligible, the electrons turn into hot electrons (the electron temperature is larger than the lattice temperature), and the transport is characterized by the onset of ballistic transport or by velocity overshoot phenomenon [ÖAL+05, SN07].

For low electric field, Albrecht *et al.* [ARL+99] predicted, using Monte Carlo simulation, an electron mobility of undoped single crystalline ZnO to be about $300\,\mathrm{cm^2V^{-1}s^{-1}}$ at room temperature. In practical terms, the charge carrier mobility in ZnO is conventionally extracted using Hall effect, which gives insights into the carrier concentration and its type. The highest bulk mobility of a single ZnO crystal at room temperature was extracted to be about $205\,\mathrm{cm^2V^{-1}s^{-1}}$ with a carrier concentration of $6 \cdot 10^{16}\,\mathrm{cm^{-3}}$ [LRS+98, LHS99]. Due to carrier freeze-out effect, at 8 K the conduction is mainly determined by hopping effect. Above this temperature a combination of band conduction and hopping occurs, whereas above 40 K band conduction is dominant and at 50 K a mobility peak value of about $2000\,\mathrm{cm^2V^{-1}s^{-1}}$ is observed, as validated theoretically and experimentally by [LRS+98]. Nevertheless, depending on the growth technique, on the crystalline orientation used for the ZnO crystal or film, and on the defect density, the charge carrier mobility at room temperature is reduced. It varies from below $100\,\mathrm{cm^2V^{-1}s^{-1}}$ to around $150\,\mathrm{cm^2V^{-1}s^{-1}}$ [IFN+00, MSKY02, EFI03, KLW+03].

For high electric fields, Monte Carlo simulations were also used to predict the drift velocity versus electric-field characteristics for bulk ZnO [ARL+99]. The first change (lower increase) in the drift velocity at room temperature occurs at $50\,\mathrm{kVcm^{-1}}$, and a peak value of $3 \cdot 10^7\,\mathrm{cms^{-1}}$ is observed at $250\,\mathrm{kVcm^{-1}}$; increasing the electric field further leads to a decrease of the drift velocity [ARL+99]. Commonly, these high electric fields are not achieved during device operation; however, with the device scaling down to the

submicron range, transient transport may occur at the gate dielectric interface of a field-effect transistor, as observed in Si-based MOSFETs [ÖAL+05, SN07].

The previously discussed electron transport characteristics were extracted and analyzed for bulk and crystalline ZnO films. For polycrystalline and nanoparticulated films, grain boundaries have a strong influence on the charge carrier transport. Considering the nanoparticulated film from Figure 2.5, which is formed by spherical shape nanoparticles, the charge carriers that are above a threshold depth (d_T) are free to flow through the film, whereas the ones under this depth are considered trapped [OMNH08, OH10]. The carrier concentration at the interface can be influenced by the application of a transversal electric field, as the one applied when a gate electrode is used in a conventional field effect transistor structure (discussed in the next subsection). Additionally, due to the interaction with the atmosphere and to the interface states, the nanoparticle surface is commonly depleted [MFN+04, Kli07, PFN+16]. Therefore, the electron flow through a nanoparticulated film is affected by the barrier energy at the interface between neighboring nanoparticles and by the internal grain structure and carrier concentration of the nanoparticle [MFN+04, HNT+04]. The charge carrier transport through grain boundaries induces the formation of a nanoparticle network; thus, the film depicts paths with high and low impedances [Meu99]. The mechanisms that govern the electron flow in the film are the tunneling through the barrier (direct or Fowler-Nordheim [Jen03] tunneling), the thermionic emission, the Frenkel-Poole emission [Fre38a, Fre38b, TO93], the hopping effect, and the space-charge-limited current conduction [Chi14, Wol11]. The voltage and temperature dependences of each transport process are used experimentally to identify the main mechanism responsible for the charge carrier transport [SN07]. Wolff has reported, using a vertical structure, that the electron transport mechanism in ZnO nanoparticulated films is mainly determined by Frenkel-Poole emission for low electric fields, and by space-charge-limited current conduction when the applied electric field is increased [Wol11]. Nevertheless, the transport mechanism strongly depends on the treatments performed on the nanoparticulated film, such as annealing processes, on the chemical stress suffered during the integration process, as well as on the film morphology, such as grain boundaries density and nanoparticles characteristics.

For the transistor integration, ZnO precursors and ZnO nanoparticle dispersions have been used. The main characteristics regarding the integration process, as deposition methods, chemical reactions (for the ZnO precursors) or fabrication processes (for the nanoparticle dispersions), and material characterization are reported in Section 3.2. Due

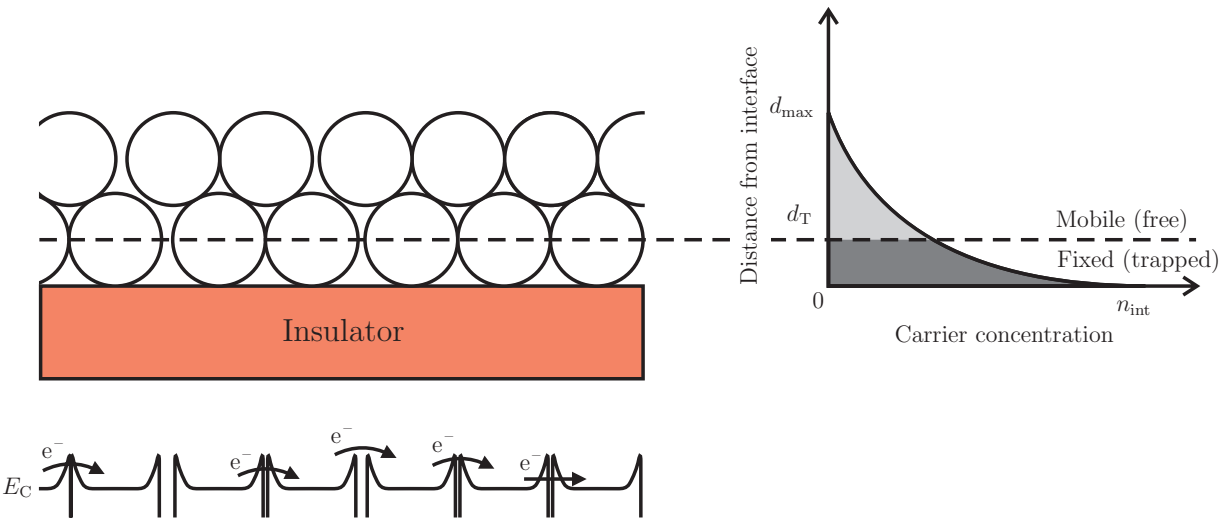


Figure 2.5: Schematic model of the interface between a nanoparticulated (spherical shape) semiconducting film and an insulator (gate dielectric). The charge carrier flow through the nanoparticles and which carriers are trapped or free regarding the nanoparticle size are shown. Adapted from [MFN+04, OMNH08, OH10].

to the transport mechanism through a non-crystalline film, there are favorable current paths (percolation paths) in the semiconducting film. Hence, trap activity at specific current paths may lead to a discrete fluctuation of the transistor current. The origin of this effect and its influence in the transistor's electrical characteristics are discussed in Section 4.2.1.

2.2 TFT Principles, Operation and Characterization

In this section, the main aspects regarding TFT operation are discussed. First, the metal-semiconductor contacts are presented; they affect the TFT electrical characteristics and are responsible for the injection of charge carriers into the semiconductor. The discussion is followed by the TFT operation modeling and finally the TFT electrical characterization with the main electrical parameters as well as the methods used to characterize the transistors integrated in this study.

2.2.1 Metal-Semiconductor Contacts

The operation of the TFTs is strongly affected by the interface between the drain/source electrodes and the active semiconducting layer and its properties. The drain and source electrode material is crucial to determine whether electron or hole injection is favored. The charge carrier injection is determined by the position of the materials' Fermi level with respect to the valence/conduction bands for inorganic semiconductors and to the frontier molecular orbitals[1] for organic compounds. In this study, the materials used for the integration of the drain and source electrodes are metals, as they allow an increased device current density and a reduced interconnection resistance between different transistors, a requirement for circuit integration [SN07]. Since the theory of metal semiconductor systems is extensive and its discussion is not the main focus of this dissertation, only essential aspects and characteristics, relevant to this study, are presented. The main discussion covers the contact between a metal and an n-type material (ZnO is used as active semiconductor in the TFT integration) and the effects and nonlinearities that influence the TFT operation. An in-depth discussion on the topic can be found, for instance, in references as [SN07] and [RW88].

After both materials, *i.e.* the metal and the semiconductor, are put in contact, the formation of a barrier at the interface occurs, as shown in Figure 2.6. This barrier is formed due to the exchange of charges (built-in potential) between the materials in order to equilibrate the Fermi levels. Thus, the metal-semiconductor contact acts as a single system. The current transport and the contact characteristics are based on the behavior of this barrier [Pie96, SN07].

The intrinsic barrier height ($q\phi_{\mathrm{Bn0}}$) − metal to an n-type semiconductor − is defined by the difference between the metal barrier height, or work function ($q\phi_{\mathrm{m}}$), and the electron affinity[2] ($q\chi$) from the semiconductor. However, in the presence of an electric field (also without bias due to the build-in potential), the barrier energy for charge carrier emission is lowered. This effect is called image-force lowering or Schottky effect [Rid78]. The barrier reduction is smaller than the barrier itself; on the other hand, the barrier depends on the

[1] Frontier molecular orbitals describe the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) for organic materials [BL07, Sir14].

[2] The electron affinity in a semiconductor is measured from the bottom of the conduction band (E_{C}) to the vacuum level.

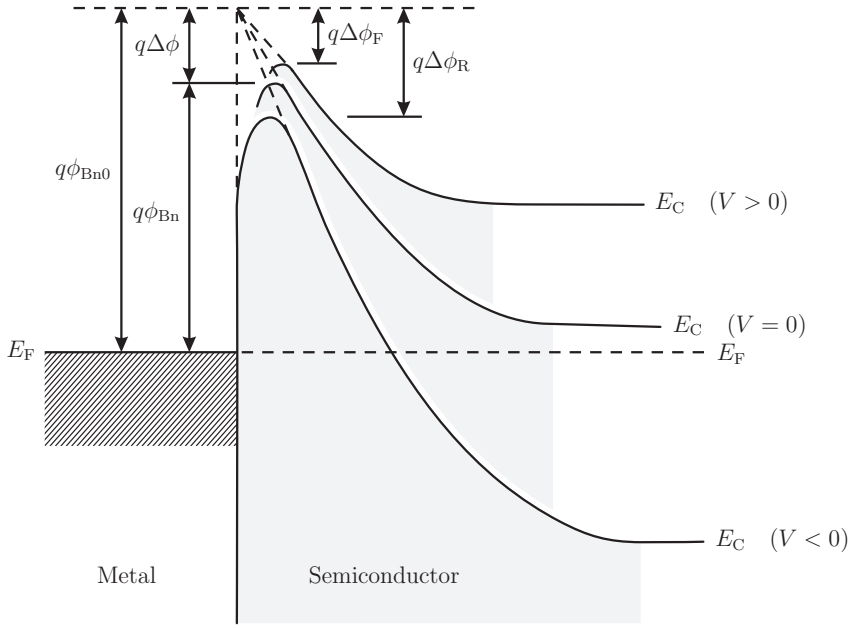


Figure 2.6: Energy-band diagram of a metal and an n-type semiconductor contact under different biasing conditions considering the Schottky effect.

applied voltage. The image-forced lowering of the barrier height ($\Delta\phi$) can be observed in Figure 2.6 and can be expressed as:

$$\Delta\phi = \sqrt{\frac{q\mathscr{E}_m}{4\pi\epsilon_s\epsilon_0}} \tag{2.1}$$

with $\mathscr{E}_m$ as the electric field at the interface and $\epsilon_s\epsilon_0$ as the permittivity characterizing the semiconductor medium. Depending on the bias applied to the metal-semiconductor contact, a variation on the image-forced lowering is observed. When a positive bias is applied to the semiconductor, the contact is under forward bias and the barrier energy for the carriers located in the semiconductor is lowered, increasing the charge carrier injection. The barrier energy for the carriers located in the metal is, due to the Schottky effect, higher ($\Delta\phi_F < \Delta\phi$) as the applied voltage has opposite effect to the build-in potential. Under reverse bias (negative voltage applied to the semiconductor), the barrier energy is lower ($\Delta\phi_R > \Delta\phi$) for the charge carriers in the metal and higher for the carrier in the semiconductor. The width of the barrier is also affected by different bias states, as depicted in Figure 2.6. The depletion region of a contact under forward bias is narrower than of a contact under reverse bias; nevertheless, the upper part of the barrier is wider for contacts under forward bias. This modulation of the barrier width influences the charge

carrier injection through a tunneling process, which will be discussed further in this work as this effect is an important aspect of the TFT operation.

Additionally, the behavior of the metal-semiconductor contact is affected by interface states present in the semiconductor and by surface contamination, which shift the formed barrier. This pinning effect can, in some cases, affect the barrier in such manner that the barrier height is almost entirely defined by the interface states of the semiconductor. It is known that this effect is stronger in semiconductors with covalent bonds, such as gallium arsenide (GaAs), in which the barrier characteristics are essentially independent of the metal work function. For ionic semiconductors, such as aluminum nitride (AlN), the barrier height is strongly dependent on the metal work function [KMM69]. In this study, nevertheless, ZnO has been used in the TFTs fabrication process and, as prior discussed, the ionicity of ZnO resides at the borderline between covalent and ionic compounds [ÖAL$^+$05, Kli07]. Therefore, the effect of the metal work function in the metal-semiconductor barrier is not well-known. Additionally, when ZnO nanoparticles are used, the barrier is also affected by the high density of interface states and by defects existent in nanocompounds [YLPC07, ZDZC09].

The current transport mechanism through a metal-semiconductor contact under forward bias is depicted in Figure 2.7. The current flow through the barrier is mainly defined by the majority charge carriers and not by the minorities as in p-n junctions. The main mechanisms are:

(a) Emission of electrons from the semiconductor over the top of the barrier into the metal;
(b) Quantum-mechanical tunneling through the barrier;
(c) Recombination in the space-charge depletion region;
(d) Recombination in the neutral region ("hole injection" from the metal to the semiconductor).

The emission of electrons over the barrier (a) is the most important mechanism; the others are considered as deviation from the ideal behavior [RW88]. Nevertheless, the combination of the mechanisms (a) and (b) is partially responsible for the TFT operation characteristics. The applied voltage modulates the barrier width (Figure 2.6) affecting the probability of charge carriers tunneling through the barrier. Figure 2.8 depicts in detail the combination of the charge carrier flow over and through the barrier. Charge carriers with enough energy (higher than the metal-semiconductor barrier height) flow over the barrier

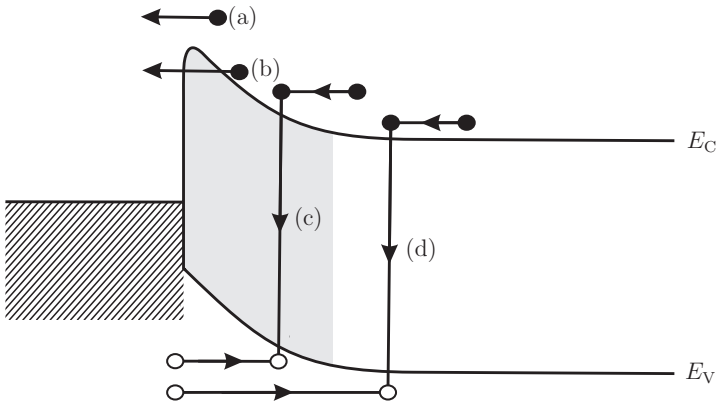


Figure 2.7: Charge carrier transport mechanisms through a forward-biased metal-semiconductor contact.

(thermionic emission). Charge carriers near the conduction band are field-emitted (tunnel-effect) through the barrier if all the requirements for the tunneling process are achieved, *i.e.* tunneling probability, occupation probability in the semiconductor and unoccupied probability in the metal are satisfied. The combination of effects − thermionic (over the barrier) and field emission (through the barrier) − is nothing more than the tunneling of thermally excited charge carriers through a thinner (upper) part of the barrier. When the barrier is under reverse bias, the tunneling current and the thermionic assisted tunneling current through the barrier can be much larger because the barrier width is reduced in the upper part, as depicted in Figure 2.8. Additionally, a reversed biased contact allows a higher electric field drop increasing the tunneling effect [PS66].

The total current density considering both the thermionic and field emissions can be expressed as:

$$J = J_o \left[\exp\left(\frac{qV}{\eta kT}\right) - 1 \right] \tag{2.2}$$

where J_o is the saturation current density, V is the applied voltage, η is the ideality factor, q is the elementary electric charge, T is the temperature and k is the Boltzmann constant.

For systems where the current flow is exclusively defined by the carrier transport over the barrier, the saturation current density is determined by the thermionic emission theory[3] and the ideality factor is close to unity. However, when the tunneling process starts

[3] Saturation current density defined by the thermionic emission theory: $J_o = A^{**}T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right]$ with the effective Richardson constant (A^{**}) taking into account the recombination velocity and the probability which an electron has to cross the barrier [Pie96, SN07].

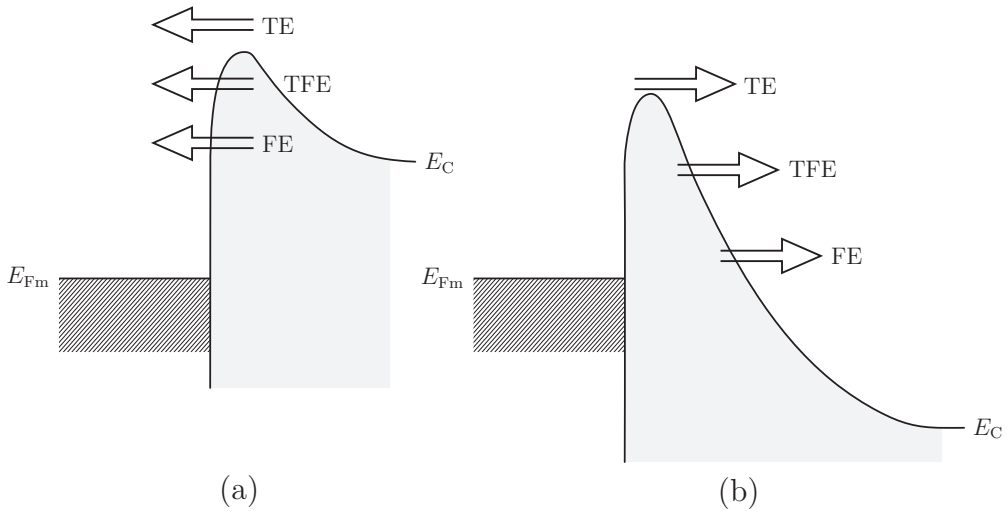


Figure 2.8: Energy-band diagram depicting qualitatively the field-emitted (FE), the thermionic-emitted (TE) and the thermionic-field emitted (TFE) charge carriers (a) through a forward-biased and (b) through a reverse-biased metal-semiconductor contact.

to occur, the saturation current density and the ideality factor increase rapidly [PS66]. For Si-based contacts exposed to high temperatures (charge carriers energy is larger than the barrier height) and with low doping levels, the carrier transport over the barrier is the main effect responsible for the current flow. Nevertheless, when low temperatures and high doping levels are used, the tunneling process is the dominating effect in the device. Depending on the doping level and on the applied voltages the contact behaves as a low impedance ohmic contact comparatively to the semiconductor resistance. For these contacts, the main mechanism for current flow is tunneling through the barrier; thus, the barrier height is negligible.

2.2.2 TFT Modeling

In this subsection, the main characteristics of the TFT are presented, as well as a basic model to understand its behavior and the differences when compared to conventional MOSFETs. As discussed before, the characteristics of the transistors integrated in this study are affected by the metal-semiconductor contacts; there are two of these contacts: one at the source electrode and another at the drain electrode. The schematic band diagram of an unbiased TFT at thermal equilibrium is depicted in Figure 2.9a. The barrier height ($q\phi_{Bn}$) from the metal to the n-type semiconductor for the electron transport is also shown. As no bias is applied to the device, there is no current flow. By applying positive

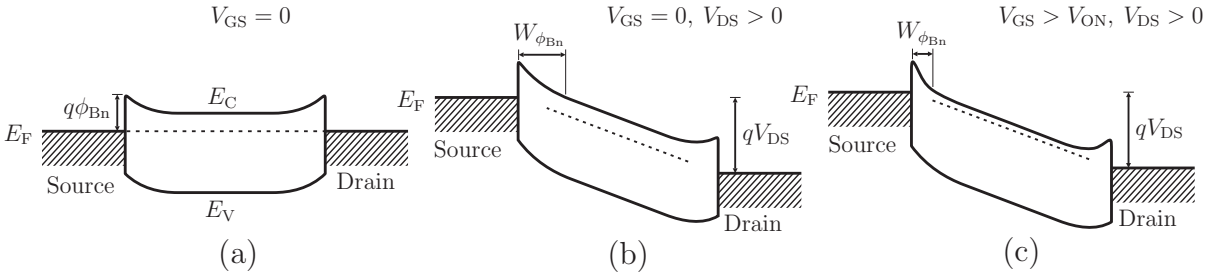


Figure 2.9: Schematic energy-band diagram along the TFT considering the metal-semiconductor contact at the drain and source electrodes: (a) without applied voltages; (b) with drain voltage; and (c) with drain and gate voltages.

drain voltage, the lowering of the drain electrode potential is expected; in this way, the metal-semiconductor contact at the source electrode is reversed biased and the one at the drain electrode is forwarded biased. As explained before, the charge carrier transport in the metal-semiconductor contacts also depends on the barrier's width ($W_{\phi_{Bn}}$); if the barrier width at the contact is thin enough, there is the possibility of charge carriers tunneling through it. Ideally, however, no current flows through the device in this condition, as the barrier is sufficiently wide to suppress carrier tunneling (Figure 2.9b). Nevertheless, by applying a positive gate voltage, the n-type semiconductor is brought into accumulation mode. The increase of the carrier concentration is, for the metal-semiconductor contacts, similar to a higher doping level in the semiconductor. This effect reduces the barrier width, increasing the probability of charge carriers tunneling through it, thus increasing the device current flow (Figure 2.9c). This accumulation-mode operation is a distinguished feature of the TFTs integrated in this study when compared to conventional MOSFETs. While in a conventional MOSFET the transistor channel is in inversion mode − *i.e.* an NMOS device is fabricated using a p-type semiconductor material − the TFT operates in accumulation mode − *i.e.* an n-type device is fabricated using an n-type semiconductor material.

The charge carrier flow in metal-semiconductor contacts during the TFT operation can be modeled as a contact resistance at the drain and source electrodes. This resistance is affected, for instance, by the materials used and by the active contact area between the semiconductor and the metal. Also, the contact characteristics are affected by the bias applied to the electrodes. This effect can be modeled through a shift of the voltage at which the transistor is assumed to start to conduct. The consideration of contact resistances for the metal-semiconductor contacts is plausible and it is consistent with

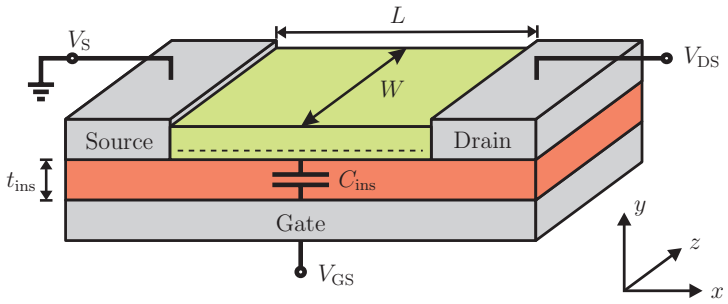


Figure 2.10: TFT schematic base structure used for the modeling.

experimental characterizations. Moreover, it allows a more direct modeling and electrical characterization of the TFTs.

The modeling of a TFT considers the basic device structure shown in Figure 2.10. The following assumption are taken to simplify the derivation of an analytical model:

– The electric field along the semiconducting layer (component x) and the electric field perpendicular to the semiconductor (component y) are independent;

– The charge carrier mobility is constant along the channel (all induced charges are due to free carriers);

– The total transistor current is dominated by the drift current;

– The charge in the channel varies linearly with respect to the applied gate voltage;

– The device is large enough that short channel effect, *e.g.* drain-induced-barrier lowering, can be neglected.

The device can be modeled as a simple capacitor ($C = Q/V$) and the charge carrier concentration in the transistor is proportional to the voltage drop across the insulator as:

$$q\Delta n(x) = C_{\text{ins}} \left[V_{\text{GS}} - V(x)\right] \tag{2.3}$$

where $q\Delta n(x)$ is the gate-induced charge density, C_{ins} is the gate capacitance per unit area, V_{GS} is the gate voltage and $V(x)$ is the channel voltage along the channel at a distance "x" (x is 0 at the source electrode and equal to L at the drain electrode). The current through the device, *i.e.* drain current (I_{D}), can be expressed as:

$$I_{\text{D}} = W q \mu \left[n_{\text{o}} + \Delta n(x)\right] \mathscr{E}(x) \tag{2.4}$$

where W is the channel width, μ is the charge carrier mobility, $\mathscr{E}(x)$ is the electric field along the channel and n_{o} is the initial charge carrier density in the semiconductor. Combining both equations and integrating them for the whole device (transistor length $-$ L) the following equation is achieved:

$$I_{\mathrm{D}} = \frac{W\mu C_{\mathrm{ins}}}{L}\left[(V_{\mathrm{GS}} - V_{\mathrm{ON}})V_{\mathrm{DS}} - \frac{V_{\mathrm{DS}}^2}{2}\right], \quad (V_{\mathrm{DS}} < V_{\mathrm{DSAT}}) \tag{2.5}$$

with the turn-on voltage (V_{ON}) defined by Hong *et al.* [HYC+08], which takes into account the density of free charge carriers (n_{o}) and the thickness of the accumulation layer in the semiconductor (h). The turn-on voltage (analogous to the threshold voltage in conventional MOSFETs) is expressed by:

$$V_{\mathrm{ON}} = -\frac{qhn_{\mathrm{o}}}{C_{\mathrm{ins}}}. \tag{2.6}$$

Equation 2.5 is only valid when $V_{\mathrm{GS}} \geq V_{\mathrm{ON}}$ and $V_{\mathrm{DS}} < V_{\mathrm{GS}} - V_{\mathrm{ON}}$, *i.e.* the transistor is not operating in the saturation regime. Commonly, this operation state is defined as the transistor linear region. When the applied drain voltage is comparable to the gate voltage ($V_{\mathrm{DS}} = V_{\mathrm{DSAT}} = V_{\mathrm{GS}} - V_{\mathrm{ON}}$), the voltage drop at the drain electrode falls to zero and the conducting channel is pinched off; hence, the transistor is under saturation regime. In this state, the transistor current becomes independent of the applied drain voltage, and the following equation is derived:

$$I_{\mathrm{DSAT}} = \frac{W\mu C_{\mathrm{ins}}}{2L}\left(V_{\mathrm{GS}} - V_{\mathrm{ON}}\right)^2, \quad (V_{\mathrm{DS}} \geq V_{\mathrm{DSAT}}). \tag{2.7}$$

The above derived expressions provide a base model for the device operation and supply the reader with the basic concepts for understanding the key elements of the TFT operation. The differences and discrepancies between the TFT behavior and this model are considered as deviations from the ideal behavior. Additionally, these equations are similar to the MOSFET ones with the main variation being related to the definition of the threshold voltage (V_{T}), or in the case of TFT, of the turn-on voltage (V_{ON}). For MOSFETs, the conducting channel is formed by an inversion layer, hence the threshold voltage is defined as the gate voltage beyond flat-band just starting to induce an inversion

charge sheet[4] [SN07]. The turn-on voltage is defined as the voltage when an appreciable drain current starts to flow through the transistor extracted from the $logI_D - V_{GS}$ transfer curve. V_{ON} is defined at the point where there is enough accumulated charge carriers at the semiconductor/gate dielectric interface allowing a current flow through the device terminals (drain and source). The procedure used to characterize the TFT integrated in this study is discussed in Section 2.2.4.

2.2.3 TFT Non-Idealities

In the previous section, the TFTs were modeled assuming an ideal device. However, due to the low-temperature processes used in the transistor integration as well as the use of low-cost production methods, the device depicts a high density of charge traps and non-idealities. For example, the contact resistance between the semiconductor and the drain/source electrodes, and the non-crystalline layer of the semiconductor limit the flow of charge carriers in the device, restraining its performance. The main non-idealities are discussed here; nevertheless, more information regarding this topic can be found in [HYC+08, Con10].

As already mentioned, one of the effects that limits the TFT performance is the contact resistance between the drain/source electrodes and the semiconducting layer. Unfortunately, due to the non-ideal metal-semiconductor contacts usually present in these devices, an accurate estimation of the contact resistance value is complicated to be achieved. The contact resistance depends on the contact area between both materials, which is influenced by the TFT setup (discussed in detail in the next section); on the interaction with the atmosphere; and on the presence of traps and impurities at the interfaces. Even with the hindrances encountered in the extraction of the contact resistance, its effect, however, can be observed in the electrical characteristics of the transistors, which provides a qualitative estimation of the contact quality. Figure 2.11 depicts simulated $I - V$ curves of an ideal transistor with different contact resistances at the drain and source contacts. The increase of the contact resistance induces a reduction of the drain conductance ($\delta I_D / \delta V_{DS}$) and leads to a reduced drain current level in the output characteristic. This effect occurs because the TFT is biased at a lower effective voltage due to the voltage drop at

[4] The traditional definition of V_T related to a particular band-bending condition in MOSFETs has a historical background. Modern MOSFETs affected by non-idealities and by the whole technology advancements and modifications consider a more operational concept of the transistor threshold [OCGSM+13].

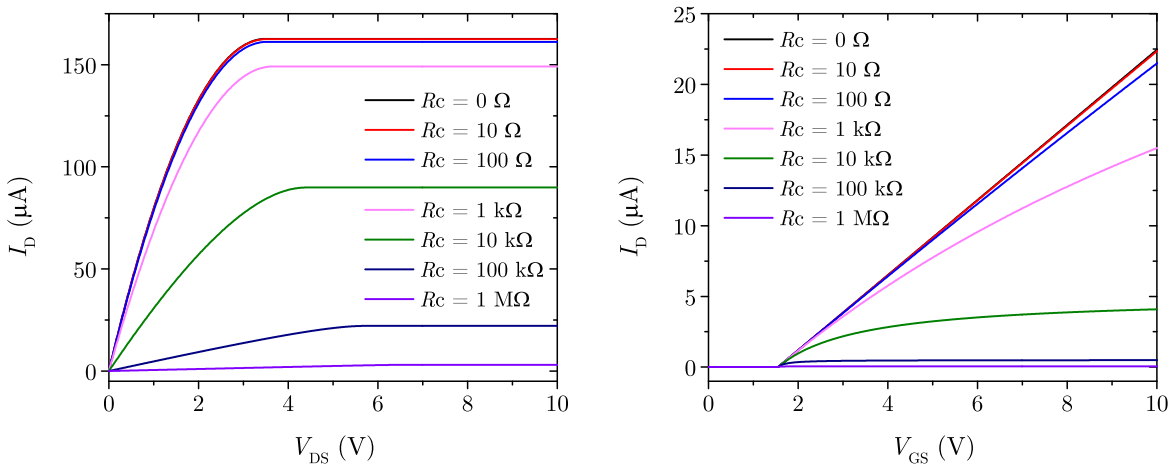


Figure 2.11: Effect of the contact resistance at the drain and source electrodes on the TFT (a) output (with $V_{GS} = 5\,V$) and (b) transfer (with $V_{DS} = 0.1\,V$) characteristics. The simulation was performed using an ideal TFT with series resistance ($R_C = R_D = R_S$) varying from $0\,\Omega$ to $1\,M\Omega$ (TFT parameters: $V_{ON} = 1.5\,V$, $\mu = 5\,cm^2V^{-1}s^{-1}$, $L = 5\,\mu m$, $W = 500\,\mu m$ and $C_{ins} = 5.31 \cdot 10^{-6}\,Fcm^{-2}$).

the series resistances (metal-semiconductor contacts). Additionally, the drain voltage at which the channel pinch off occurs is increased. Also, if not properly accounted for, the reduction of the current level due to the increased contact resistance causes the extracted mobility to be underestimated. On the one hand, the contact resistance is small compared to the resistance imposed by the semiconducting layer in wide band gap inorganic-based TFTs [HYC+08, Fra15]; on the other hand, with the scaling of TFTs and with a reduced contact area between the drain/source material and the active semiconductor, an increase of the contact resistance effect is expected. A more complex model, accounting for the non-linearities introduced by these contacts, can be achieved by including diodes to the equivalent transistor model [NSGJ00, Hor04]. Figure 2.12 depicts equivalent circuit models of the TFTs considering the contact resistance.

The semiconductor properties also induce instabilities and non-idealities to the TFT behavior. In the previous derivation, it has been considered that the entire semiconducting layer (variation on the charge carrier density) is controlled by the applied gate voltage. Conversely, depending on the layer thickness and its morphology, just parts of the layer are controlled by this electric field. The semiconducting layer interface opposite to the gate electrode can be affected (depleted or accumulated) by an interaction with other materials (substrate or passivation layers) or, in the case of non-encapsulated inverted transistor

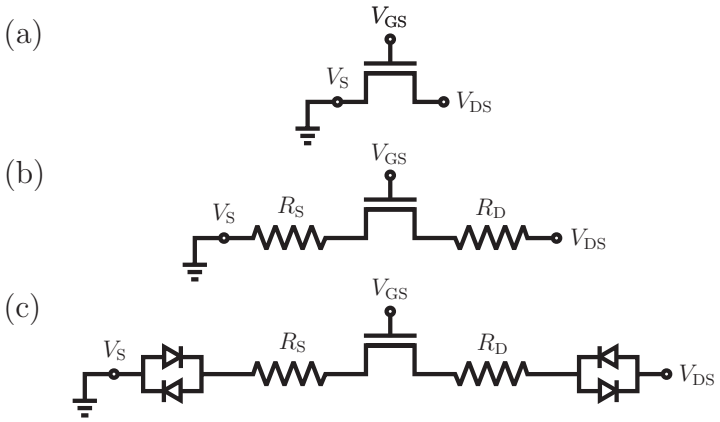


Figure 2.12: Equivalent circuit (a) of an ideal TFT, (b) considering contact resistances at the drain and source electrodes, and (c) accounting non-linearities of these contacts.

setups, with the ambient atmosphere. Therefore, the charge carrier density in the semiconductor is also defined by these interactions. The inner part of the film which is not affected by the applied gate voltage, or by the interaction with the ambient or with other materials can be considered as a bulk material. As a consequence, the active semiconducting layer can be modeled as a three layer material, as shown in Figure 2.13. Since this film is usually thin (up to 100 nm) and the semiconductor presents low intrinsic conductivity, the effect of the bulk layer can be neglected when compared to the interface layers. In the case of nanoparticulated semiconductors, due to the nanoparticle morphology even when a thicker layer ($200 - 300$ nm) is used, the bulk layer does not affect the transistor behavior significantly. Besides the film's porous character, the large active surface area of nanocompounds enhances the interaction with other materials and with the ambient, thus the whole film can be influenced by the interface layer opposite to the gate electrode. As a result, the inner part of the layer is also commonly neglected. In Section 4.2, this interaction as well as the procedures to mitigate its effects are further discussed. A simple way to model the effect of the semiconductor thickness and its interaction with the ambient and with other materials is the addition of a resistance in parallel to the ideal TFT. For instance, in the case of a high conductive semiconductor with appreciable thickness, this additional resistance is small, causing the transistor current to increase with increment of drain voltage; thus, no current saturation is observed. Additionally, a higher transistor current in the cut-off regime is modeled by this resistance. One of the drawbacks of this model is the inability to cover the case when the formation of the accumulation channel is affected by the interaction with the ambient air. An example of this effect is when the entire ZnO layer is depleted due to the adsorption of oxygen, and no accumulation layer

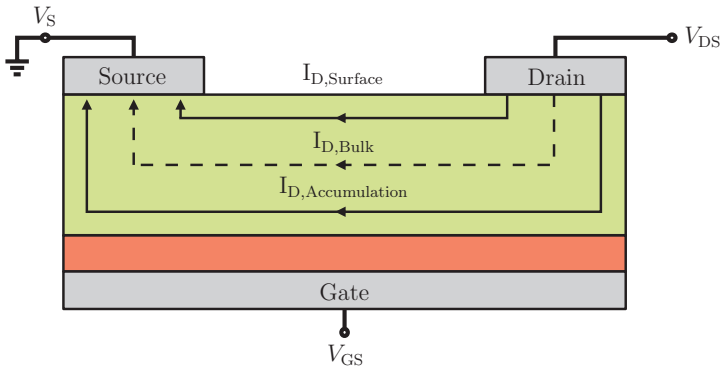


Figure 2.13: TFT schematic model considering three different conducting paths in the semiconducting layer.

can be formed [XFH+12, BSTS12]. At this point the semiconducting layer thickness and the transistor setup are critical factors [MAH+08, TBS+11, BPM+06]. Films as thin as 15 nm are strongly affected by the atmosphere [MAH+08, BPM+06].

Up to this point, the effect of charge carrier trapping and its consequences have not been considered. Nevertheless, the emission and capture of carriers by traps influence the transistor behavior and performance. The main effects on the transistor's electrical characteristics are the shift of the turn-on voltage and the variation on the density of charge carrier in the accumulation layer of the semiconductor. Additionally, the trapping of charge carriers is reported to induce a hysteretic behavior in the transfer curve depending on the gate voltage sweep direction [FBJ+09, SS05, WH11, Wol11]. Conjointly, the electron transport in TFTs commonly occurs through a non-crystalline layer; thus favored conduction paths (percolation paths) are formed and, depending on the trap position and activity, the current flow is reduced or even blocked in the specific path [Meu99]. A more detailed explanation and derivation of the current transport and of the trap activity effects on the transistors integrated in this study, especially for nanoparticulated semiconducting layers, are presented in Section 4.2.1.

The assumption that the accumulation layer induced by the gate voltage is formed exactly at the interface between the semiconductor and the gate dielectric is also not entirely correct. Actually, the accumulation layer extends itself over some nanometers and even over a few monolayers for organic-based TFTs [Hor04]. For nanoparticulated semiconducting films, the channel thickness is proportional to the nanostructure size. This consideration is attributed to the contact between neighboring nanoparticles and to the energy required by the charge carriers in the accumulation layer to flow through the film.

In this case, a tradeoff between the particle size and the extension of the accumulation layer defines the transistor characteristic. Smaller particles lead to a high number of interconnections increasing the semiconducting layer resistance. The extension of the accumulation layer required for the charge carrier flow, however, is reduced. The formation of an accumulation layer in nanoparticulated films is also influenced by the temperature, by the electric field and by the trap density of the film, as discussed previously in Section 2.1. The effect of the accumulation layer thickness can be modeled as a capacitance in series to the capacitance of the gate dielectric, hence the effective gate capacitance (C_{G}) is reduced as:

$$C_{\mathrm{G}} = \frac{C_{\mathrm{ins}} C_{\mathrm{sem}}}{C_{\mathrm{ins}} + C_{\mathrm{sem}}} \tag{2.8}$$

where the capacitance of the gate insulator per unit area (C_{ins}) can be modeled as a parallel plate capacitor:

$$C_{\mathrm{ins}} = \frac{\epsilon_{\mathrm{ins}} \epsilon_0}{t_{\mathrm{ins}}}. \tag{2.9}$$

with ϵ_0 as the vacuum permittivity, ϵ_{ins} as the permittivity of the insulator and t_{ins} as the thickness of the insulator. As the charge carrier distribution on the accumulation layer and the potential drop through the semiconductor depend on the semiconductor morphology and its characteristics, the capacitance of the semiconductor per unit area (C_{sem}) can be calculated by integrating the induced charge carrier density in the accumulation layer ($q\Delta n(y)$) and the voltage drop on the semiconductor ($V(y)$). The integration is limited by the semiconductor/gate dielectric interface (t_{int}) and by the thickness of the semiconducting layer (t_{sem}):

$$C_{\mathrm{sem}} = \int_{t_{\mathrm{int}}}^{t_{\mathrm{sem}}} \frac{q\Delta n(y)}{V(y)}\, dy \tag{2.10}$$

In practical terms, the thickness of the gate dielectric is in general much larger than the accumulation layer, and the majority of the charge carriers are located at the gate dielectric/semiconductor interface. As a result, the gate capacitance is essentially defined by the properties of the gate insulator. Therefore, the charge carrier distribution on the semiconducting layer overestimates the gate capacitance of the TFT model and causes the charge carrier mobility to be underestimated. The modeling of the extension of the accumulation layer and its effect on real devices were deeply investigated by Horowitz [Hor04]. Additionally, the carrier accumulation depends on the TFT setup, as discussed in [FBJ+09] and in the integration process chapter (Section 3.1).

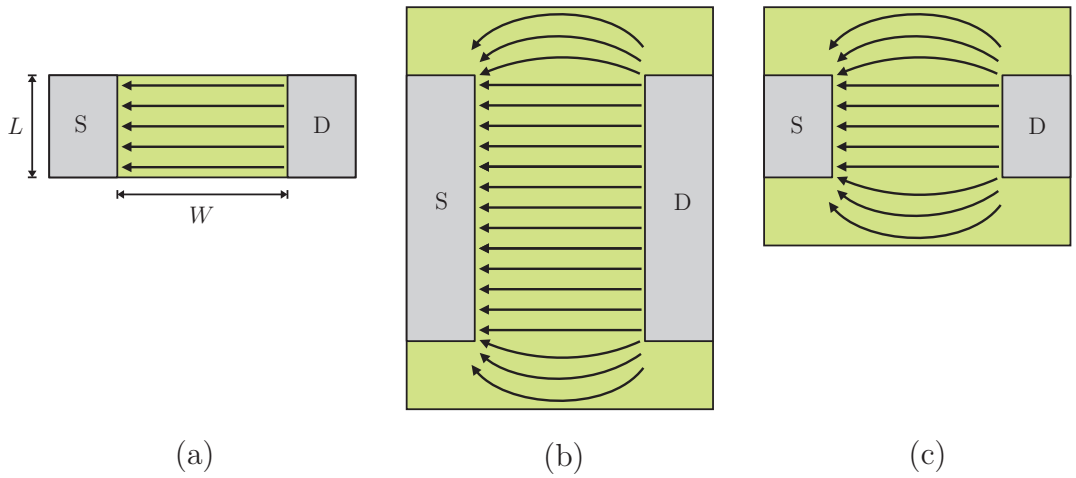


Figure 2.14: Fringing current – Schematic layout of a TFT structure (S = source electrode, D = drain electrode, gate electrode and gate dielectric layers are not explicitly shown here), in which (a) the channel layer is patterned, (b) the channel layer is unpatterned with a high W/L ratio, and (c) the channel layer is unpatterned with a low W/L ratio.

The charge carrier mobility has been considered constant for the TFT modeling, even though there are several indications that the mobility is not constant in the accumulation channel. The interface roughness between the gate dielectric and the semiconductor, electron trapping, velocity saturation, and charge carrier transport through a non-crystalline material are examples of mechanisms that scatter the charge carriers. This points to a non-uniform and non-constant carrier mobility; instead, the mobility can vary depending on the applied voltages, either drain or gate voltages. As a consequence, different types of mobilities are defined as well as different extraction methods [Hof04, Sch06, JP06]. In the next section, the procedure used to extract the charge carrier mobility from the transistors integrated in this work is derived.

Frequently, to simplify the integration process, the semiconductor and the gate electrode are not patterned. Depending on the width-to-length ratio of the TFTs, an overstated quantification of the device current is observed. Figure 2.14 depicts the current flow in devices with patterned and unpatterned semiconducting layers. For devices with unpatterned layer and low width-to-length ratio, the peripheral (fringing) current increases significantly the device current. This effect may cause the carrier mobility to be overestimated, and it presents an issue in the validation of the transistor performance as the mobility is strongly affected by the transistor geometry. Based on this assumption, a direct comparison with transistors metrics published by other groups is not a straight forward task, and discrepancies are often observed.

2.2.4 TFT Characterization

This section discusses the methodology used to characterize the transistors integrated in this study. In order to avail a comparison with transistors integrated by different groups a standardization is required. However, no specific standard regarding the characterization of inorganic TFTs or nanoparticle-based transistors is available. For this reason, the transistor characterization is based on the 1620-2008 IEEE-standard [IEE08] for organic transistors, and on the procedure proposed by Hoffman [Hof04] and Hong *et al.* [HYC+08] for the characterization of thin-film transistors. Nevertheless, due to the operation similarities between TFT and MOSFET devices, the transistor characterization is also based on the standard characterization procedures of silicon-based transistors.

The main characteristics of TFTs are the transfer ($I_D(V_G)$) and output ($I_D(V_D)$) curves[5]. Another important aspect is the behavior of the leakage current through the gate electrode during the extraction of both curves. These characteristics avail the extraction of the metrics used to analyze the TFT performance and to compare different transistors. The main metrics are: the turn-on voltage, V_{ON} (or the threshold voltage, V_T); the current modulation, I_{ON}/I_{OFF}; the subthreshold swing, S; and the charge carrier mobility, μ.

The transistor's electrical characterization was performed using a HP-4156A – Precision Semiconductor Parameter Analyzer and a Karl Süss microprobe station equipped with Süss MicroTec PH100 micromanipulators with tungsten probes (Model: 72T-J3/70x1.2" from American Probe & Technologies, Inc.) for the contact between the transistor's pads and the measurement equipment. The measurements were made under ambient atmosphere in a dark environment with relative humidity in the range of 25-60 %. The hold and delay[6] times are fixed to 150 ms. Variations in the electrical setup or in the procedure are discussed for each particular case.

Turn-on voltage and threshold voltage

As TFTs are basically devices controlled by the application of electric fields with similar functional behavior to MOSFETs, the extraction and use of the threshold voltage is largely employed. There are different methods for its extraction [Sch06, OCGSM+13].

[5] Since the source electrode is always assumed to be grounded the V_G, V_D, I_G, I_D notations have the exactly same meaning as V_{GS}, V_{DS}, I_{GS}, I_{DS}.

[6] Parameter of the HP-4156A which defines the wait time after the applied voltage or current step before starting the measurement.

The linear extrapolation of the $I_D - V_G$ plot for non-pinched channels (commonly when low V_D is applied) or of the $I_D^{1/2} - V_G$ plot for pinched channels (high applied V_D), the V_G at a specific drain current, and the transconductance method are examples among other methodologies for the extraction of the threshold voltage. As the TFTs characteristics frequently deviate from the ideal behavior, the extraction method of V_T results in a large ambiguity in the obtained values. Depending on the fitting parameters used for the linear regression or on which point the curve is extrapolated, for example, a large variation in the extracted values is observed. Another source of uncertainty on the determination of the threshold voltage is the equations (transistor model) used for the derivation of the method, which are often based on an ideal device.

The use of V_{ON} avoids the ambiguity in the definition or in the extraction method of V_T, because V_{ON} is simply the V_G in which the transistor drain current starts to increase in the $log(I_D) - V_G$ plot. As discussed previously, this method indicates the applied gate voltage on the onset of the accumulation layer when the current through the device starts to flow. Figure 2.15 depicts the extraction of the V_{ON} as well as the extraction of the V_T using linear extrapolation. To standardize the extraction of the V_T, the point of the curve that is extrapolated is the one in which the maximum transconductance is observed. Nevertheless, because of the TFT non-idealities, this point is not always clear, and a small variation of its location may incur in a considerable error.

Even with the simple extraction method and definition of V_{ON}, the extracted values are influenced by leakage currents and by the measurement system. These disturbances affect the transistor off-state current and thus cause the extracted V_{ON} to shift. For instance, when the transistor gate leakage is high (compared to I_D), a positive shift of V_{ON} is often observed. Notwithstanding, depending on the magnitude of the leakage currents, the transistor operation is affected leading to an incorrect extraction of all metrics and not just of V_{ON}. For the characterization of the TFTs integrated in this study, V_{ON} is the main parameter defining the conditions in which the transistor starts to conduct. However, in order to allow a comparison with other studies in the literature, the V_T (extracted using the linear extrapolation) is mentioned.

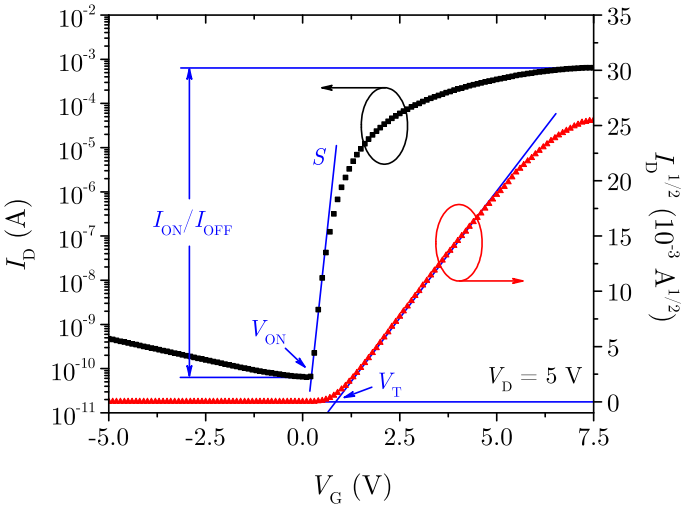


Figure 2.15: Transfer curve depicting the extraction difference of the V_{ON} and V_T. Additionally, the extraction procedure of the I_{ON}/I_{OFF} ratio and the subthreshold swing (S) are shown.

I_{ON}/I_{OFF} ratio

The I_{ON}/I_{OFF} or $ON\text{-}OFF$ ratio is the ratio between the maximum and the minimum drain current extracted from the TFT transfer characteristic ($log(I_D) - V_G$ plot), as depicted in Figure 2.15. The maximum current is in general limited by the semiconductor material properties, by the contact quality between the semiconductor and the drain and source electrodes, and by the capacitive coupling quality between the gate electrode and the TFT channel. The minimum current is determined by leakage currents and by the measurement setup. Both the maximum and the minimum currents are influenced by the TFT dimensions and design [WS09]; for example, long channel TFTs ($50 - 100\,\mu$m) have a proportional higher current than short channel TFTs, as the contact resistance at the drain and source electrodes are small compared to the semiconducting layer resistance. The off current is also affected by the TFT layout. While long channel TFTs possess a larger gate area ($W \times L$), hence a larger leakage current through the gate electrode, the reduction of the channel length increases the drain-to-source leakage current as the electric field between drain and source is inversely proportional to the channel length at constant V_D.

For electronic switches applications, high I_{ON}/I_{OFF} ratios are necessary and values around $10^4 - 10^6$ are usually required [WS09].

Subthreshold swing

The subthreshold swing (S) indicates how effective the device is able to turn-on and turn-off. This metric is also extracted from the $log(I_{\mathrm{D}}) - V_{\mathrm{G}}$ plot (see Figure 2.15) as:

$$S = \left.\frac{\delta V_{\mathrm{G}}}{\delta log I_{\mathrm{D}}}\right|_{min}, \tag{2.11}$$

and it indicates the necessary V_{G} to increase I_{D} by a decade. In practical terms, a low subthreshold swing is desired, as the device requires less gate voltage excursion to be turned from a fully off to a fully on state, or vice versa [WS09]. The subthreshold swing metric is often related to the transistor trap density and to the gate dielectric/semiconductor interface quality [Wol11, Sch06].

Field-effect mobility

The charge carrier mobility is frequently cited as one of the most important performance metrics to compare different devices, as it directly influences the device's maximum operation frequency and its range of applications. High mobility devices present a faster switching response and a higher drain current, which avails a faster charge and discharge of the circuit's capacitances. The extraction of the charge carrier mobility can be performed through different approaches. The method used in this study is the field-effect mobility (μ_{FE}) due to its extraction simplicity and to its widespread use in the literature. Moreover, this metric is the one indicated in the IEEE standard 1620-2008 [IEE08], where the mobility value of the majority carriers of semiconductor materials is reported in $\mathrm{cm^2V^{-1}s^{-1}}$. The field-effect mobility is extracted according to:

$$\mu_{\mathrm{FE}} = \frac{L g_{\mathrm{m}}}{W C_{\mathrm{ins}} V_{\mathrm{D}}} \tag{2.12}$$

where g_{m} is the transconductance defined as:

$$g_{\mathrm{m}} = \left.\frac{\delta I_{\mathrm{D}}}{\delta V_{\mathrm{G}}}\right|_{V_{\mathrm{D}}=constant}. \tag{2.13}$$

This extraction method has the advantage of disregarding the use of V_{T} avoiding the ambiguities concerning its definition. Although the μ_{FE} is used by different groups, this

method is sensitive to contact resistances and neglects the effects of V_G in the formed channel layer [Sch06].

Other extraction methods, such as the effective mobility (μ_{eff}), require the use and definition of the channel charge density, as well as the use of V_T, which introduces considerable error and ambiguity to the mobility values. Additionally, the μ_{eff} extraction method is also affected by the contact resistance. On the other hand, the saturation mobility (μ_{sat}) is less sensitive to this resistance; however, the transistor channel pinch off causes the transistor length to vary. Conjointly, μ_{sat} neglects the gate voltage influence on the mobility and applies a correction body effect factor that is not well-known [Sch06].

The previously mentioned mobility extraction methodologies have a historical background as they are used for the characterization of MOSFET. Moreover, other methods and corrections regarding the charge carrier mobility are found in the literature [Sch06, HYC+08]. Hoffman [Hof04] has proposed the average mobility (μ_{avg}) and the incremental mobility (μ_{inc}), which provide insights into the TFT behavior enclosing its non-idealities. The μ_{avg} yields to the average mobility of the total charge carrier concentration in the induced channel for $V_{GS} > V_{ON}$, and the μ_{inc} provides insights into the mobility of the carriers added or removed from the accumulation layer for a small variation of V_G [Hof04]. The use of such mobility definitions has gained attention in the scientific community; in the future their employment should be considered.

CHAPTER 3

INTEGRATION

In the previous chapter, the fundamentals of TFTs were discussed with emphasis on device operation and working principles. The current chapter is related to the integration of these devices. First, different setups of TFTs are presented, highlighting the advantages and disadvantages of each structure. Secondly, the description of the integration process is divided considering each integration step or layer for the achievement of a complete transistor or device. Particular focus is given to material properties and characteristics as well as to integration techniques used in this work; nevertheless, a brief discussion concerning other methods and materials is also exposed.

3.1 TFT Setups

The arrangement of the basic components of a TFT, *i.e.* semiconductor, dielectric and metal contacts (gate, drain and source), has a strong influence on both the device performance and the integration process itself. Commonly, the TFTs are divided into four groups of setups:

- inverted staggered (Figure 3.1a)
- inverted coplanar (Figure 3.1b)
- staggered (Figure 3.1c)
- coplanar (Figure 3.1d)

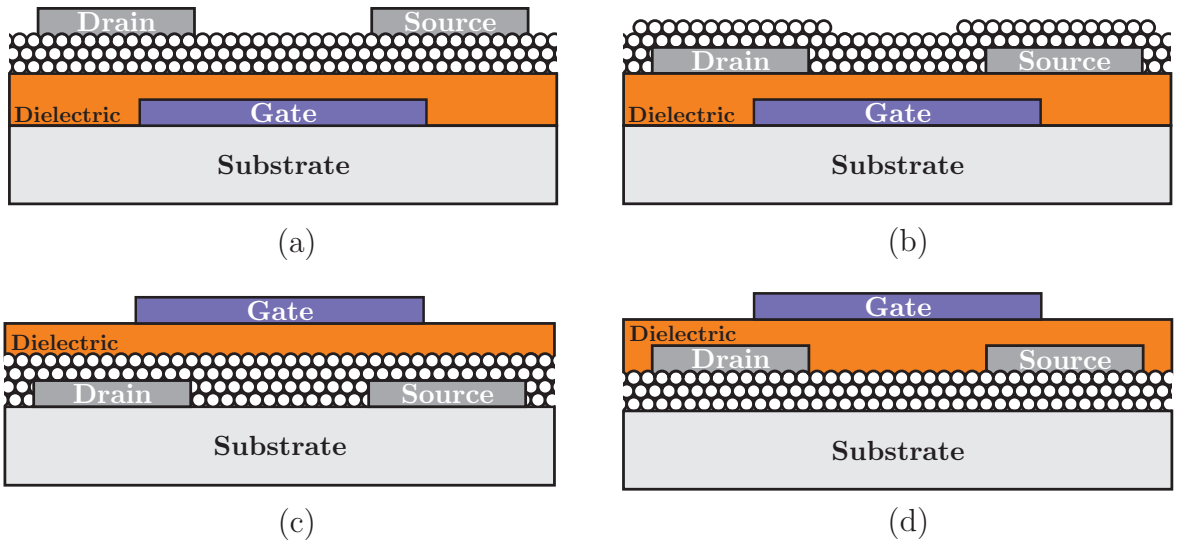


Figure 3.1: General TFT setups, including: (a) inverted staggered, (b) inverted coplanar, (c) staggered and (d) coplanar.

The two aspects that define the setup are (I) the position of the gate electrode regarding the drain and source contacts and (II) the position of the drain and source electrodes and the gate dielectric relatively to the position of the channel in the active semiconductor. If the gate electrode is located below the drain and source contacts (closer to the substrate), as shown in Figure 3.1a and Figure 3.1b, the structure is called bottom-gate or inverted. When the gate is above the line of the drain and source electrodes, the conventional setup is also called top-gate or non-inverted (see Figure 3.1c and Figure 3.1d). In staggered structures, the drain and source electrodes and the gate dielectric are placed at opposite sides using the channel as reference, *i.e.* the drain and source electrodes are not in the same plane as the conductive channel. If they are in the same side (plane), the setup is defined as coplanar.

In order to evaluate other materials (*e.g.* new semiconducting or dielectric materials) or variations on integration techniques (*e.g.* an improved deposition of the nanoparticle dispersion or surface treatments), usually bottom-gate setups are applied using either the silicon wafer as a gate electrode or a metal layer without the definition of the gate electrodes, as shown in Figure 3.2. This approach reduces the integration time as well as the template complexity. When a silicon wafer is used as gate electrode, the wafer can be oxidized in order to obtain a high quality oxide as gate dielectric. In this manner, the instabilities related to the gate dielectric can be avoided because of the well-known electrical characteristics and growth techniques of SiO_2 [Hil14, Jae02]. Nevertheless, the

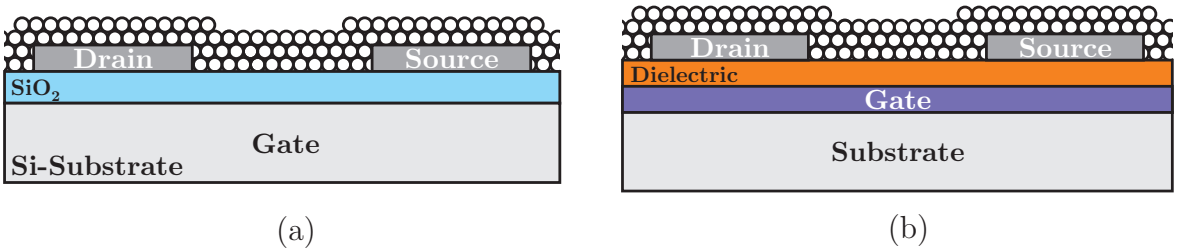


Figure 3.2: Inverted coplanar TFT structures: (a) using Si/SiO_2 as gate electrode and gate dielectric, and (b) using a non-structured metal layer as gate electrode. This technique can also be applied in inverted staggered setup.

usefulness of the wafer as gate electrode is only justified for preliminary experiments. With the objective of integrating circuits with multiple TFTs, the non-structuration of the gate electrode is inadequate as one gate electrode controls all the devices. Additionally, the large overlap area between the top layer and the gate electrode significantly increases the gate leakage currents and disturbs the TFT electrical characteristics. This overlap is in great part defined by the drain and source electrodes and the pads required to establish the contact between the measuring probes and the TFT electrodes.

The setup choice strongly depends on the materials and processes used for the TFT integration. The research community and the industry favored the use of top-gate structures for the fabrication of poly-Si TFT due to the high temperatures required during the crystallization process of the semiconductor. Using these setups, the subsequent materials used for the TFT integration as well as the interfaces are unaffected by the deposition process of the poly-Si [Tho84, KA03]. When amorphous Si (a-Si) is used as active semiconductor, however, lower temperatures are required for the deposition [Kat99, Hil14] allowing different setups. Nonetheless, laser annealing techniques and alternative low-temperature processes have also expanded the use of poly-Si as active semiconductor in TFT technology [LTK+91, SSM93, UI01]. In order to avoid the light induced disturbances on the TFTs used in LCDs, which are constantly illuminated by the display back light, inverted staggered structures were applied using the bottom gate electrode as a light shutter [Tho84, Kat99].

For the integration of metal-oxide and of organic semiconductor based TFTs, the use of bottom-gate (inverted) setups dominates, with just a few groups researching top-gate structures [FBD+13, MNO+13, WFHL+15]. These setups are used due to the low chemical and physical stress suffered by the semiconductor during the integration process. For organic-based TFTs, inverted coplanar structures are favored when photolithographic

techniques are employed, as the semiconductor deposition is the last step in the transistor integration process, hence the semiconducting layer is not affected by any other processes [Sir14]. This setup is used for the integration of inorganic-based TFTs as well [FBM12, PMV+16]. However, the main drawback of this structure is the relative high resistance between the semiconductor and the drain and source contacts due to the low contact surface area between both materials. This effect is highlighted when nanoparticulated semiconducting films are applied, because of the spherical shape of the nanostructures [Wol11]. Figure 3.3a depicts the limited contact between a nanoparticulated film and a metal contact. For organic-based semiconductors, the growth behavior is affected by the abrupt change of the underlying layer. The contact quality between the semiconductor and the electrodes can be improved when the drain/source material is deposited on top of the active semiconductor (Figure 3.3b). For a nanoparticulated semiconductor, the gaps between the particles are filled up increasing the contact surface between both materials. On the one hand, inverted staggered setups improve the contact quality between the drain/source electrodes and the semiconductor, increasing the charge carrier flow through the contact. On the other hand, the electrodes are not in direct contact with the conductive channel and the charge carriers have to flow through the semiconducting layer thickness until the formed channel is reached, as shown in Figure 3.4. This path can be modeled as an access resistance, and this effect is a characteristic of staggered structures. Conversely, the access resistance is reported to be negligible in comparison to advantages of the improved contact area between the drain/source and the semiconductor [PCNF04, BL07]. As the deposited semiconductor commonly presents unconformities, such as valleys, peaks and pin holes, the charge carrier path to reach the channel is reduced, decreasing the access resistance [BL07]. For coplanar setups, the access resistance is also negligible as the drain and source electrodes are in direct contact with the formed accumulation layer.

Due to the better contact between the semiconductor and the drain and source materials, staggered setups are popular; nevertheless, especially for organic semiconductors, the structuration of the electrodes is done by shadow masks, which avoids any chemical contamination of the semiconductor. The use of a shadow mask, however, limits the minimum transistor size to about $10 - 20\,\mu$m, though a higher resolution has been reported by [AKZ+12, ZRL+13]. On the other hand, the mask and alignment procedures are complicated and time intensive. Moreover, in order to achieve better depositions and higher resolutions, the shadow mask must be in contact with the sample, which increases

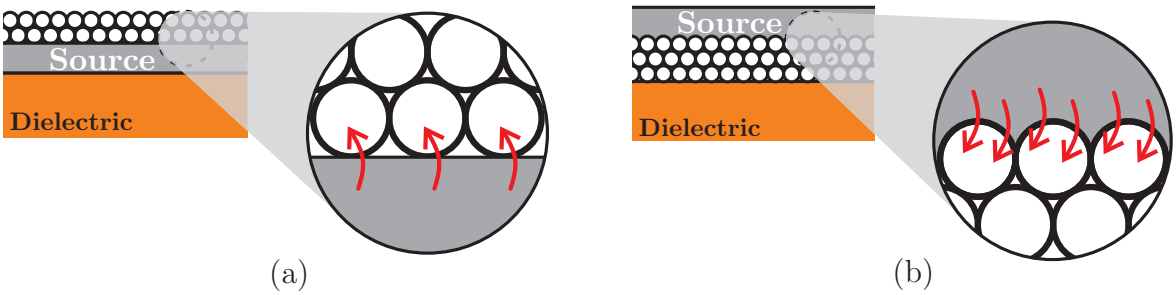


Figure 3.3: Detail of the contact between the source (drain) electrode and the nanoparticulated layer in (a) inverted coplanar and (b) inverted staggered setups showing the charge carrier injection.

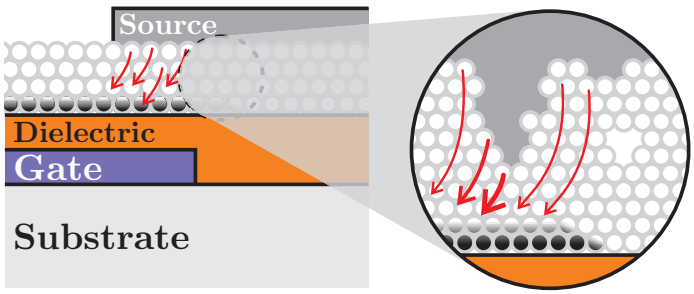


Figure 3.4: Access resistance observed in staggered setups, which has its origin on the path that charge carriers have to flow through the semiconducting layer thickness to reach the formed accumulation layer. Due to unconformities in the semiconducting layer, the path until the channel is reduced and the access resistance is commonly negligible.

the possibility of damaging the underneath layer. Furthermore, for large-scale production and for circuits with a high density of elements, the use of shadow masks are not entirely suitable. For this reason, the use of photolithography is the standard method to achieve high resolution and high transistor densities. It should be noted, however, that if the semiconductor is not stable against the chemicals used or no passivation (etch stopper) is applied, the semiconductor can be damaged, decreasing the device performance.

Another aspect of the setups is the interaction of the semiconductor with the ambient air. In this case, both inverted staggered and inverted coplanar devices are degraded by this interaction if no stabilization of the layer or passivation is applied. This opens up the opportunity to evaluate different treatments for the semiconducting layer, as well as the evaluation of the TFT as a sensor [DSZ+15, YSLY16]. Conjointly, for inverted setups, the semiconductor is deposited on the gate dielectric; therefore, they have to be compatible. This concern is enhanced when solution-based techniques are used, as a good wetting between both materials is required. Moreover, both materials have to be also chemically compatible, *e.g.* the semiconducting solution should not etch or damage the layer underneath. Mainly for nanoparticle dispersions the interface between the gate dielectric and the nanoparticulated film presents empty spaces [Wol11] which reduce the capacitive coupling between the gate electrode and the active semiconductor. For a better capacitive coupling through the filling of the gaps between the semiconductor and the dielectric layer, conventional structures are preferred. These setups also have the advantage of using the gate insulating material and the gate electrode as a semiconductor passivation layer mitigating its interaction with the ambient. However, the main drawback of top-gate setups is the increased roughness at the gate dielectric/semiconductor interface when nanoparticulated or uneven semiconducting films are used. As a result, the improved capacitive coupling between the gate electrode and the transistor channel is jeopardized by the roughness and instabilities at channel interface limiting the charge carrier flow and reducing the transistor performance [FBJ+09].

In this study, based on the improved interface between the active semiconducting layer and the gate dielectric as well as on the results achieved by [Wol11], inverted TFT setups were applied. Due to the better contact quality between the drain and source electrodes and the semiconductor material, the staggered version was preferably chosen. However, in order to identify and minimize instability effects in the transistor operation (Section 4.2), inverted coplanar structures were also employed; as in this case, chemical and physical stresses endured by the semiconducting layer during the drain and source electrodes struc-

turation are avoided. In this way, different ZnO deposition methods and solution-based materials could be evaluated. Conjointly, this setup was also applied for the developing of the stabilization of the nanoparticulated film by UV irradiation and wet-air treatment, as described in Section 4.2. Here, the materials and methods used for each component (semiconductor, gate dielectric, contacts and substrates) of the transistors are firstly discussed, whereas the integration procedure of the TFT itself is addressed in the last subsection.

3.2 Semiconductor

In this subsection, the main characteristics and deposition methods regarding the semiconductor used in this study are presented. As the intrinsic properties of the ZnO were already discussed in Section 2.1, the discussion presented here focuses on the integration process itself. Conjointly, the deposition methods available and commonly used in the literature are briefly addressed.

Besides the electrical characteristics of the semiconductor, its chemical and physical properties should also be considered. The semiconducting compound has to endure the stresses imposed by the integration process without degrading its attributes. Generally, the requirements are related to the deposition quality, and to the compatibility with the entire integration process and with further materials employed in the device. The temperature required during either deposition or later annealing steps should be, for instance, compatible with the dielectric layer and with the substrate. Moreover, the formation of a reliable semiconducting layer is also a primary concern. Therefore, for the low-cost sector, it is important to develop an efficient integration process which is robust and reproducible. High performance devices just achieved under strict conditions are shaded by cost-efficient techniques. In this case, the main goal is not the performance itself, but rather the tradeoff between cost, robustness, and performance. Furthermore, complex inorganic compounds with addition of Ga, In, Sn to the ZnO crystal structure improve the transport quality and the charge carrier mobility [ÖAL$^+$05, FBM12], although increasing the system's complexity and budget. Doping of the ZnO is also used to achieve better charge carrier mobilities [KYK14, FBM12], though it increases production costs and introduces instabilities in the process and in the transistor behavior.

In this study, ZnO is used as the semiconductor for the TFT integration. To maintain the costs as well as the system and integration process complexity under a certain level, the

employment of ZnO was investigated primarily without addition of any extra compounds. Notwithstanding, several deposition techniques for ZnO as active semiconducting layer are available; and even limited to solution-based processes, there are still many alternatives that can be employed. Aiming at the low-cost sector and a later high-scale production the main focus is given to such deposition methods, hence some of them are investigated and discussed here. Nevertheless, methods using vacuum techniques and semiconducting materials employing different compounds are also briefly addressed.

3.2.1 Deposition Methods

The main advantage regarding vacuum techniques is the compatibility with the current manufacturing processes encountered in the microtechnology. The know-how developed over decades has driven these processes also into the integration of TFTs. Vacuum-based systems generally deposit dense and high quality films with a good adhesion to the substrate. They are widely used, for instance, in the production of flat-panel displays, and among them the sputtering technique is the most mature one [PMKP12, FBM12]. Nonetheless, other techniques, such as ALD [PHJ$^+$08, LKKP07], plasma or UV enhanced ALD [LCH$^+$10, LKK$^+$10, NLKK14], and pulsed laser deposition (PLD) [SWDM07, GCBT13], are also utilized to achieve high quality layers. The advantages of sputtering techniques are mostly related to the material choice, as it is possible to deposit a wide range of compounds by adequate selection of the target. Additionally, this sort of deposition is commonly performed at room temperature and by controlling the power and pressure, there is the opportunity to optimize the layer quality [BPG$^+$09, FBM12]. Another feature is the use of reactive sputtering processes, in which the amount of oxygen in the chamber can be controlled adjusting the oxygen content of the metal-oxide semiconductor [TMSM99, HQH$^+$05]. More complex techniques, as co-sputtering using multiple targets, can be performed for the achievement of complex material compositions as GIZO, for instance [BPG$^+$09]. ALD techniques provide conformal and dense films [LKKP07, PHJ$^+$08], however, due to the slow process and to the susceptibility of failures caused by variations on the chemicals and on the system, the use of these methods are not entirely suitable for flexible electronics.

The fabrication of devices using solution-based methods offers the possibility to replace vacuum processes with cost-efficient techniques. Besides the drastic reduction in the production cost through the employment of high throughput continuous processes, the

substrate size is not anymore limited by the vacuum system, *e.g.* by the chamber size. By applying solution-based materials, mature techniques, as the ones used in printed media, as well as new deposition methods can be used. However, TFTs integrated using such processes at temperatures adequate for flexible substrates, generally depict inferior electrical performance in comparison to the ones deposited under vacuum conditions. Here the tradeoff between production expenses and performance has to take the application requirements into consideration. Although the employment of solution-based processes in TFT technology is relatively recent, it has already demonstrated an impressive evolution regarding performance and reliability, as well as manufacturing aspects [KYK14, DSBM14, PMV$^+$16]. Depending on the deposition method applied, *e.g.* printing, the number of photolithographic or shadow masks can be minimized reducing costs. Moreover, solution-based processes are not confined only to the deposition of metal-oxide-semiconducting layers; other semiconductors (*e.g.* organic-based) as well as organic-inorganic hybrid systems also profit from these techniques. The discussion presented here, however, focuses on the materials used for the TFT integrated in this study. The materials can be found dissolved in the form of a precursor or dispersed in the form of nanoparticles in a solvent. Both solution types were evaluated during this work and are described in the following subsections.

Concerning the deposition itself, there are different methods to achieve continuous and structured films. They can be divided according to the principle behind each deposition technique, though sometimes there may be overlap between the groups. Figure 3.5 shows the main groups.

The principal deposition methods employing solution-based materials are:

I) Drop-casting: This deposition method is characterized by the deposition of a drop of the solution on the substrate and subsequent vaporization of the solvent. Due to the uneven solvent evaporation in the drop, generally there are cracks in the film, and the distribution of the semiconductor is uneven [ZAK$^+$11, FBM12, LLS12, KYK14]. The process can be improved by addition of thermal or mechanical (vibration) energy, by tilting the substrate, by surface treatments or by controlling the solvent evaporation in a sealed chamber or under inert gas purging [ZAK$^+$11]. Additionally, in order to induce a regular evaporation, droplet-pinning technique can be used [ZAK$^+$11].

II) Spin-coating: This method is widely used by the semiconductor industry for the deposition of photoresist [Hil14]. By centrifugal forces the solution is spread onto the

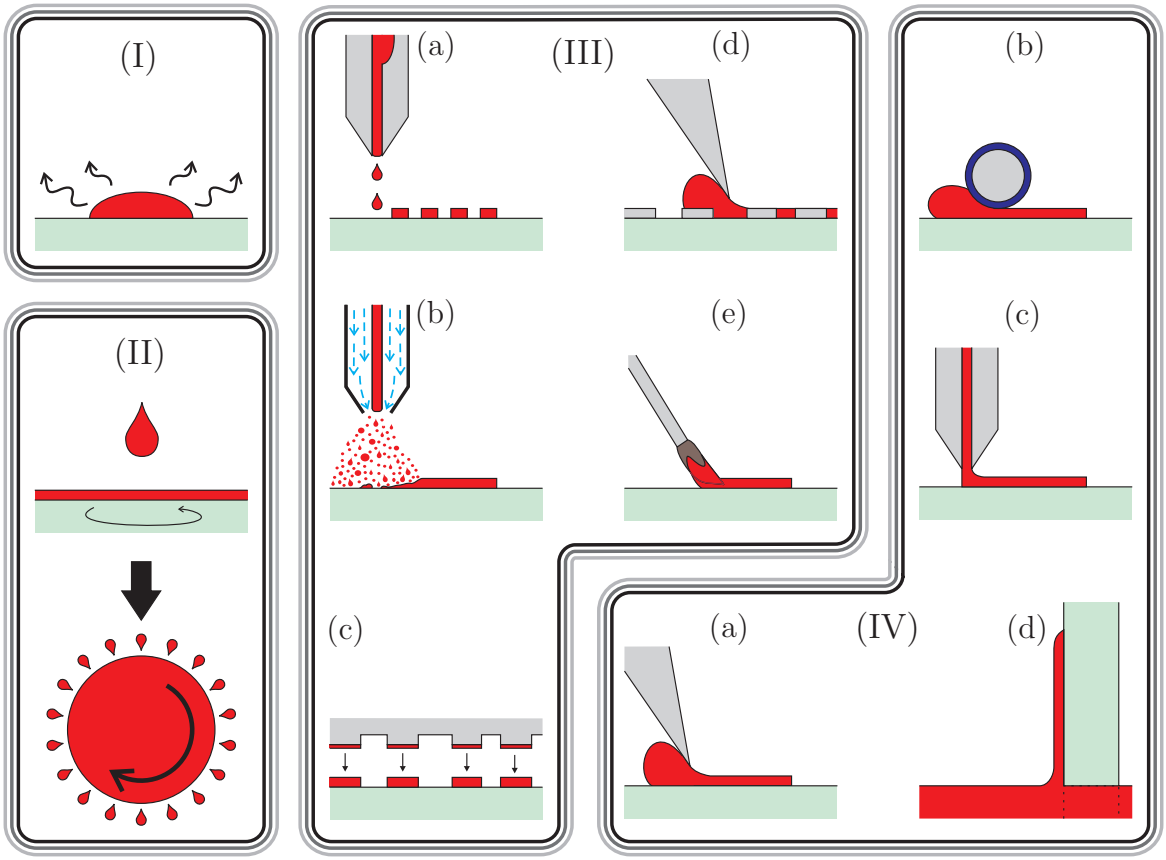


Figure 3.5: Schematic representation of the deposition methods separated in groups. (I) Drop-casting; (II) Spin-coating; (III) Printing: (a) inkjet printing, (b) spray-coating, (c) stamping, (d) screening and (e) brushing; (IV) Meniscus-guided coating: (a) doctor-blade (shearing solution), (b) Meyers rod, (c) hollow pen and (d) dip-coating.

sample, and the thickness of the layer is affected by the spin speed as well as by the solution concentration, viscosity and temperature. This technique is also extensively employed for the deposition of solution-based (in)organic materials. For organic semiconducting solutions, off-center methods have shown some promising results due to the unidirectional alignment of the material [YGA$^+$14].

III) Printing: This technique can be divided in several methods. Inkjet printing, spray coating, stamping, screening and brushing are the most used principles. However, the definition of printing is sometimes merged to zone drop-casting or to meniscus-guide coating methods. In this work, printing is defined as a deposition in which the meniscus is not the main working mechanism responsible for the process, and there is no deposition of a macroscopic drop on the samples. Inkjet printing is a traditional method and its advantage is related to the absence of contact between the substrate and the machinery, and to the deposition of already patterned structures. The ejection of the "ink" (solution) is done on-demand by a piezoelectric or thermal element placed on the nozzle [Hil06]. Spray technique is similar to inkjet printing, however, in this case, the solution is ejected by a pneumatic-based system in form of droplets. These droplets are formed by aerosolization of the dispersion with pressurized air or inert gas. In the stamping technique, the solution is transported to the substrate using a stamp commonly made of a polymer (*e.g.* polydimethylsiloxane − PDMS) to avoid mechanical damage of the sample. Variation of this method, as gravure or flexographic, can also be employed to increase the process throughput [SHK13, KYK14]. Screening deposition is similar to shadow mask technique; the layer is deposited and structured based on the openings in a screen placed on top of the sample. The brushing method is a simple method which employs brushes to deposit and distribute the solution onto the sample. Especially for organic semiconducting materials, this technique is helpful as it gives an orientation for the organic crystal growth [KNJ$^+$07]. An important advantage of printing techniques is that most of its variations can be adapted to roll-to-roll processes.

IV) Meniscus-guided coating: The linear translation between the substrate and the coating tool is responsible for the deposition of the film. In this method, the solution meniscus is the main mechanism behind the deposition. Different tools or set-ups can be used to control the film thickness, orientation and quality. Doctor blade (shearing solution), implementations of Meyers' rod, hollow-pen, or a simple dip-coating into the solution are examples of processing where the solution meniscus is crucial for the film deposition. Most of these methods can also be implemented in roll-to-roll set-ups.

Another way to deposit a material is done through a chemical bath. In this case, the sample is submerged in a solution, and through a chemical reaction the material film is formed. Although it is largely used for surface coating in several industrial sectors, this method is unable to produce active TFT layers in a cost-efficient and reliable manner. Commonly, these films are porous and exhibit inferior performance compared to the films deposited by vacuum or by the previously mentioned solution-based techniques [GBKO04].

Aiming at a cost-efficient production, solution-based processes were used for the integration of the devices presented in this study. Therefore, spin-coating technique was primary used due to previous experiences and available machinery in situ. In order to avail the integration process to large area substrates, spray-coating was also used and has shown promising results, as discussed in Section 4.2. Moreover, doctor blade technique was also briefly investigated (Section 6.3) to evaluate the wide range of deposition methods that can be employed in the integration process of TFTs. An interesting fact is that between the different materials, ZnO is one of the few semiconductors that can be deposited by all deposition methods (vacuum- and solution-based). Moreover, among the binary metal-oxide semiconductors, ZnO is reported to present the highest performance with adequate carrier mobility and current modulation properties [ÖAL+05, Kli07]. These characteristics illustrate the importance of this metal oxide as a key material in the TFT technology and thus justifying its use in this work.

3.2.2 ZnO Precursors

As discussed before, one of the approaches for the active semiconducting layer fabrication is to use a precursor solution. For this method, the metal-oxide semiconductor is synthetized using a metal precursor in solvent. After its deposition on the template, the film is pre-annealed in order to remove the solvent and post-annealed to form the active semiconducting layer. During the annealing step, the main processes for the achievement of an active semiconductor are the precursor decomposition followed by a hydrolysis process where the metal is bonded to hydroxyl groups. The final step is the dehydroxylation and alloying of the film; the hydroxyl groups are removed, the metal is bounded to oxygen, and neighboring metal-oxide molecules become interconnected [KYK14]. For amorphous metal-oxide systems as GIZO and IZO, which present more than a single metal type in their chemical compositions, the same steps occur [KYK14]. However, the initial solution is a combination of all precursors. For GIZO systems, for example, the precursor contents

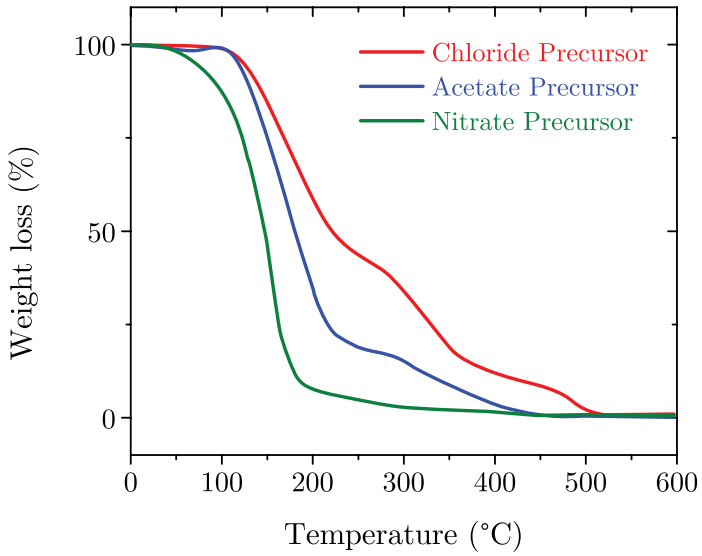


Figure 3.6: Schematic diagram of the thermogravimetric analyses of nitrate-, acetate- and chloride-based precursors. Adapted from [KYK14].

indium, gallium and zinc precursors and its electrical characteristics depend on the partial concentration of each one of them [KDS+09, JHM+10, FKD+12].

The choice of which precursor is used for the synthesis also plays an important role in the integration process itself as it influences the required annealing temperature, as well as the chemical compatibility of the solution with the substrate or with previously deposited layers. Precursors for metal-oxide systems are commonly nitrate-, acetate- or chloride-based. The temperature necessary for an adequate synthesis of the semiconductor can be evaluated by a thermogravimetric analysis. Figure 3.6 depicts a schematic diagram showing the requirements for each precursor group. Based on the synthesis temperature and on the flexible substrates limitations, acetate- and nitrate-based precursors were evaluated.

Sol-gel processes of metal-oxide compounds are commonly defined as the formation of an oxide network originated by a polycondensation of molecular precursors [HW90]. For the achievement of ZnO, commonly a zinc salt is required, and depending on its characteristics (precursor type), the reaction temperature is influenced as prior discussed. First experiments were performed employing zinc acetate ($Zn(Ac)_2$) as zinc salt. Generally the $Zn(Ac)_2$ is dissolved in an alcoholic or another organic solvent and subsequently an alkaline solution is added to it [OKY97, YI02, HFKI04]. The routine used in this study

is based on the work of Hosono *et al.* [HFKI04] in which a non-basic solution method was described for the preparation of ZnO precipitates. The general reaction is described as:

$$5\,(\mathrm{Zn(Ac)_2 \cdot 2\,H_2O}) \longrightarrow \mathrm{Zn_5(OH)_8(Ac)_2 \cdot 2\,H_2O} + 8\,\mathrm{AcH} \longrightarrow 5\,\mathrm{ZnO} + 10\,\mathrm{AcH} + 5\,\mathrm{H_2O}. \tag{3.1}$$

For the reaction accomplishment, the following chemicals were mixed. First, 5.5 g of $\mathrm{Zn(Ac)_2}$ was dissolved in 25 ml of deionized water[7]. Then, the solution was heated to 60 ℃ under vigorous stirring and, subsequently, 1.9 g of 2-methoxyethanol (2-ME) was dropwisely added to the mixture. Afterwards, water was added until the total volume of the precursor reached 50 ml. After 1 h under vigorous stirring, the aqueous solution was deposited onto the sample by spin-coating technique. It was deposited on the wafer during the low-spin phase at 800 rpm followed by a high-spin step of 3000 rpm for 30 s at room temperature. Although the high-spin phase influences the thickness of the final layer, variations from 2000 rpm to 4000 rpm have not significantly changed the electrical performance of the integrated devices. Immediately after the solution deposition, the sample was soft-baked at 115 ℃ on a hot-plate for 5 min and then baked in a convection oven at 200 ℃ for 1 h. Due to the temperature difference between the solution and the substrate during the deposition, the formation of a reliable film was not fully achieved. The deposited films possessed a high density of cracks, particles and agglomerations, and the material did not cover the whole sample. Additionally, the relative low temperature employed was not sufficient to achieve a complete synthesis reaction of the zinc acetate precursor, as already expected taking into account the thermogravimetric analysis [KYK14] and the TFTs characteristics described in Section 4.1. Moreover, in order to increase the interparticle connection quality, the solution was deposited onto a nanoparticulated film or mixed with a dispersion containing ZnO nanoparticles [LJK$^+$07, LJJ$^+$08]. The electrical characteristics of the transistors produced in this way were evaluated in Section 4.2.

Aiming at a low synthesis temperature, zinc nitrate-based precursors were used as they possess advantages regarding their thermal compatibility to flexible substrates. The precursor synthesis is based on the work of Meyers *et al.* [MAH$^+$08], where an ammine-hydroxo zinc ink for ZnO TFTs is reported. This method uses simple cation hydration chemistries and highly reactive aqueous precursors to obtain a high quality ZnO with

[7] In this study, deionized water using reverse osmosis with minimum resistivity of 18 MΩ was used in all steps and from now on the term water refer to deionized water. If for a particular reason another water type (*e.g.* distilled or non-purified) is used, the term water is clarified.

crystallization at low temperatures. Moreover, it avoids the use of metal-organic compounds, which require a high activation and diffusion energy, and employs an all inorganic hydroxo-condensation [BPS06, MAH$^+$08]. As a result of the weak acidity of the ZnO^{2+} ions, the energy required for the dehydration of the $Zn(OH)_2$ and for the oxide crystallization is much lower than for $In(OH)_3$ and $Sn(OH)_4$ [GGKL67, Sat05]. For these reasons, the fabrication of pure ZnO through this method is promising. Conjointly, the use of ammonia adds the advantage of its extreme volatility and labile bonding affording a low-temperature, rapid and low volume-loss decomposition process in comparison to other nitrogen-based ligands.

The following routine has the goal to provide a ZnO film with low impurity concentration as well as to maintain a low synthesis temperature. Due to the polarization of the NO_3^- charge cloud by acidic metal cations, the purity of the initial soluble $Zn(NO_3)_2$ is important for the achievement of a low-temperature process. For this reason, 99.998 % pure $Zn(NO_3)_2$ purchased from Alfa Aesar Co. was used. The zinc salt was dissolved in water to a total concentration of 0.5 M Zn. Under vigorous stirring 10 ml of 2.5 M NaOH was slowly added to 15 ml of the solution during the course of 5 min. The reaction can be expressed as:

$$Zn(NO_3)_2(aq) + 2\,NaOH\,(aq) \longrightarrow Zn(OH)_2(s) + 2\,NaNO_3(aq). \tag{3.2}$$

The hydroxide slurry was then centrifuged and the supernatant removed. 20 ml of water was added and stirred for 3 to 5 min, this step was followed by another centrifugation and supernatant removal. The process was repeated 5 times in order to reduce Na^+ and NO_3^- contaminations caused by incomplete reaction. After a final centrifugation, the precipitate was dissolved in 50 ml of 25 % aqueous ammonia to form the precursor as:

$$Zn(OH)_2(s) + x\,NH_3(aq) \longrightarrow Zn(OH)_2(NH_3)_x(aq). \tag{3.3}$$

Although ZnO could be dissolved directly in ammonia, a complete dissolution of large-grain ZnO powder is difficult to be achieved because of the kinetic obstacles involving the metal oxides [MAH$^+$08]. Additionally, the simple dissolution of zinc salt in ammonia also degrades the low temperature synthesis as the precursor contains non-basic counterions [MAH$^+$08]. In order to avoid this effect and to improve the dissolubility, fresh $Zn(OH)_2$ precipitates should be dissolved in ammonia. This process is already used for more than 90

years for the synthesis and purification of bulk ZnO [DJ27]. Finally, after the deposition of the precursor on the sample, the following reaction is expected:

$$\mathrm{Zn(OH)_2(NH_3)}_x\mathrm{(aq)} \longrightarrow \mathrm{ZnO\,(s)} + x\,\mathrm{NH_3(g)} + \mathrm{H_2O\,(g)}. \tag{3.4}$$

If the initial compounds are free of contaminations and the solution is properly purified during the rinse and centrifugation steps, the dehydration and oxide crystallization occur at temperatures below 100 ℃ [BAL94, MAH$^+$08] enabling the process to flexible substrates.

In order to decrease the chemical complexity and to avoid multiple steps during the centrifugation and supernatan removal, Theissmann *et al.* have proposed an alternative synthesis process [TBS$^+$11]. For this reaction, commercially available zinc oxide hydrate ($\mathrm{ZnO} \cdot x\,\mathrm{H_2O}$) was directly dissolved in ammonia. The solubility of the compound in ammonia was reported as sufficient due to the crystal water, and the final precursor solution is similar to the one previously described [TBS$^+$11]. On the other hand, this reduced synthesis process requires a higher annealing temperature or annealing in a specific atmosphere to achieve transistors with adequate electrical characteristics [TBS$^+$11, BSTS12]. To reduce contamination and to maintain the crystallization of the zinc oxide at lower temperatures for the process to be suitable to flexible substrate, this synthesis method was not applied but rather the procedure proposed by Meyers *et al.*

For the deposition of the zinc nitrate precursor, spin-coating technique was used. The stock precursor was filtered by 0.45 μm PTFE syringe filter and deposited on a steady wafer prior to the low-spin phase of the template at 800 rpm for 7 s and a high-spin step of 3000 rpm for 30 s. Immediately after the precursor deposition, the wafer was soft-baked at 115 ℃ on a hot-plate for 5 min. In order to achieve a thicker layer, the process was repeated up to 5 times. The sample was then baked in a convection oven at 150 ℃ for 1 h to ensure homogeneity and a complete crystallization of the layer.

When $\mathrm{SiO_2}$ was used as gate dielectric, the precursor has shown a good wetting to the substrate and a uniform film could be observed. By increasing the number of the precursor depositions, the layer uniformity is reduced, nonetheless the film is still homogenous. One of the drawbacks of the employment of precursors for the achievement of active semiconducting layers is the strict and necessary use of specific chemicals in its composition. As the precursor used contains ammonia and oxidation elements, the deposition of the

ammine-hydroxo zinc solution on the high-k nanocomposite (explained in Section 3.3.2) damages this dielectric. Furthermore, material agglomerations and formation of clusters on the film were also observed. This effect prevails the full use of this precursor on flexible substrates when the high-k dielectric is used without a protection layer, for instance. Additionally, as the precursor reacts with aluminum (metal used for the drain and source electrodes), the employment of different transistors setups is limited or the transistor performance is reduced due to an unstable contact between the metal electrodes and the semiconducting layer. The electrical performance of the transistors integrated using the nitrate-based precursor is discussed in Section 4.1.

3.2.3 Nanoparticulated ZnO

In contrast to the precursor approach, in which the synthesis of the semiconductor occurs on the transistor template, by employing a nanoparticle dispersion as active semiconductor material, the integration process of the semiconducting layer is divided in two main steps. First, the required nanoparticles are produced; this can be done through high-vacuum and high-temperatures processes aiming at the delivery of high-quality nanostructures. In this way, the nanoparticle fabrication is achieved by the use of high-throughput techniques which maintain low cost due to mass production [KJK$^+$02, YI02]. The second main step is the application of the nanostructures to the transistor template. Thus, the nanoparticle dispersion is deposited on the sample, followed by a low temperature process in order to remove the dispersant medium, *e.g.* water, ethanol, propylenglycol or butyl acetate. The focus of the following discussion is the employment of nanoparticle dispersions concerning the integration process. The intrinsic properties of ZnO as well as the charge carrier transport are presented in Section 2.1.

The shape of the nanostructures has a strong impact on the device performance as well as on the integration process. ZnO can be found in a wide range of different nanostructures enabling its employment in diverse fields of applications. For the integration of transistors, nanowires [GSLY05, KRA$^+$14], nanorods [TGL$^+$13, PPB$^+$16] and nanospheres [CKJ$^+$12, DGD$^+$16] are the most used structures. Due to the fact that spherical nanoparticles do not require a specific orientation regarding the transistor template, this form was chosen in this study. Nonetheless, this shape leads to the creation of percolation paths and to a high number of interparticle connections, as described in detail in Section 2.1 and 4.2.1. Additionally, as reported by [OMNH08, OH10], the size of the nanoparticles also plays

an important role in the TFT performance. On the one hand, accumulation of charge carriers at the dielectric interface may occur for large particles; on the other hand, an increase in the number of interconnection is observed in the case of small nanoparticles.

In this study, the nanoparticle dispersion used in the integration process of TFTs was chosen according to the work performed by Wolff [Wol11], where a wide range of dispersions were evaluated, analyzing the solid content in the solution, the dispersion agent, and the influence of both the annealing temperature and the atmosphere on the film characteristics. Along with the results already demonstrated by Wolff [Wol11], an evaluation of other possible dispersions was performed focusing on the deposition quality and on the density of defects (through the analyses of photoluminescence spectra of the nanoparticles). The defect density is partially responsible for the instabilities during the transistor operation, as reported in Section 4.2. The deposition of the nanoparticle dispersion (concentration about 15 wt%) was mainly conducted employing spin-coating or spray-coating using nitrogen as carrier gas. By virtue of variations in the deposition technique, as well as of the template (different gate dielectrics and treatments), each method used is described along with the proper electrical characteristics of the different groups of integrated TFTs.

The fabrication of zinc oxide nanoparticles can be done by different methods. Sol-gel processes are a common approach where the dispersion containing the nanoparticles is originated through a colloidal solution. Another method that is compatible with mass production is the synthesis in vapor gas phase with flame reactor or with coupling with microwave or electric arc [KJK$^+$02]. Other techniques include laser ablation [DKM13, GPK$^+$15, SKH$^+$15] and milling [SASM13, PZY$^+$13]. The nanoparticle used in this work are mainly fabricated by vapor gas phase and the dispersions were provided by Degussa GmbH, Nanophase Corporation Inc. and Sigma Aldrich Co.

Based on the study of Wolff [Wol11], the water-based dispersion *AdNano ZnO 20 DW* from Degussa GmbH was tested and evaluated for the integration of TFTs, because of its deposition quality and good stability (low agglomeration over time). The primary nanoparticles size is in the range of 15-30 nm of diameter, however they are generally agglomerated in 100 nm diameter clusters [Deg06]. Prior to the utilization of the nanoparticle dispersions, an ultrasonic agitation was performed in order to break down large clusters, achieving a homogeneous dispersion. A set of nanoparticles (*NanoSunguard*® from Buhler Inc.) dispersed in water, in ethanol and in butyl acetate provided by Sigma Aldrich Co. was also evaluated [Buh16]. The water-based solution possesses similar deposition quality

to the dispersion provided by Degussa GmbH. By using ethanol and buthyl acetate as solvents, the deposition wetting quality on different templates was improved; however, the film was commonly not uniform and defects were generally observed. Additionally, an improper adhesion to the sample was noted requiring a high-temperature ($> 400\,℃$) step for its fixing, therefore preventing the integration on flexible substrates. Water-based dispersions containing ZnO nanoparticles (*ZN-2650* [Nan16a], *ZN-3008C* [Nan16b], *ZN-3014A* [Nan16c]) were also provided by Nanophase Corporation Inc. While the *ZN-2650* and *ZN-3008C* demonstrated strong agglomeration issues as well as a deficient deposition quality, the dispersion *ZN-3014A* showed promising properties. It was stable over time, depicting just a slight agglomeration effect over months of storage, and showed adequate deposition quality and electrical properties. The main differences between the dispersions are the size of the nanoparticles and their fabrication procedure (coupling mechanism during the synthesis and chemicals employed) [Nan16a, Nan16b, Nan16c]. Moreover, the deposition quality of the dispersion *ZN-3014A* is slightly superior compared to the water-based dispersions provided by Degussa GmbH and by Sigma Aldrich Co., achieving a film with lower defect density. The ZnO nanoparticles from this dispersion present predominantly a spherical shape and an average diameter of around 70 nm [Nan16c].

Through photoluminescence (PL) analysis, the nanoparticle dispersions were evaluated regarding their defect density. The PL spectra of the nanoparticles are represented in Figure 3.7. For all nanoparticles samples, a drop of the dispersion was deposited on a glass microscope slide followed by a thermal treatment of 120 ℃ for 1 h in a convection oven under ambient conditions. The PL spectrum was measured at room temperature using the 325-nm line of He-Cd laser ($P = 38\,\mathrm{mW}$). The illumination intensity was determined by a Thorlabs PM100D power meter console and a CCD-camera was used as detector. The optical properties of ZnO are widely used in the literature for the evaluation of the compound quality. The two peaks observed in the spectrum are associated to the exciton recombination related to near-band edge emission (NBE) in the UV region, and to the deep-level emission (DLE) in the visible region usually observed in the presence of structural defects and impurities [ÖAL$^+$05, JP06, Kli07]. Generally, a high NBE/DLE ratio corresponds to a low density of defects in the metal-oxide structure [ÖAL$^+$05, JP06, Kli07]. From the PL spectrum analysis, it is possible to observe the difference between the structure quality of the nanoparticles, which may account for the variability in the electrical properties of the active semiconducting layer, as described in Section 4.2. Based on the electrical performance of the TFTs integrated using the water-based solution *ZN 3014A*

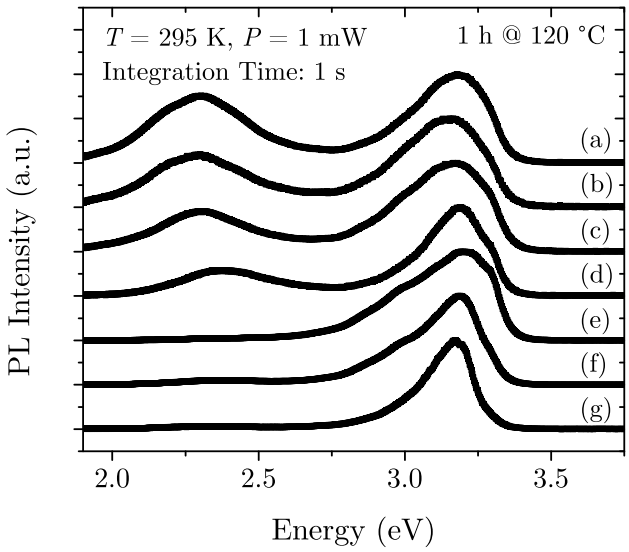


Figure 3.7: PL spectrum of the different ZnO nanoparticles dispersion including: *NanoSunguard*® from Buhler Inc. dispersed in water (a), in ethanol (b) and in butyl acetate (c), *AdNano ZnO 20 DW* (d) from Degussa GmbH, and *ZN-3014A* (e), *ZN-2650* (f) and *ZN-3008C* (g) from Nanophase Corporation Inc.

from Nanophase Corporation Inc., the influence of the temperature applied during the solvent evaporation was investigated (Figure 3.8). As expected, no significant changes in the PL spectrum were observed as no sintering process was initiated. ZnO nanoparticles require temperatures above 400 ℃ for the start of this process, as reported by Wolff [Wol11] and Lee *et al.* [LJK+07, LJJ+08]. However, the application of high temperatures are not possible when integrating devices on flexible substrate, thus they were not further investigated. It is known that a deeper characterization of the defects present in a compound can be achieved by the analysis at a few Kelvins [ÖAL+05, JP06]. Nevertheless, for the applications aimed in this study, the evaluation at room temperature has depicted adequate results for a qualitative investigation of the ZnO nanoparticles.

Besides the use of the commercially available nanoparticle dispersions, milling of ZnO powder in order to break the ZnO particle into nanoparticles was also evaluated. Therefore, a PM 100 milling machine from Retsch was used, and water and ethanol were employed as dispersion medium. However, due to agglomeration effects after the milling process as well as to the inability to achieve a homogeneous dispersion or film, this method was discontinued. Furthermore, the physical stress during the milling process produces several defects on the compound that require a high-temperature annealing step to avoid instabilities issues for a later use as active material in transistors.

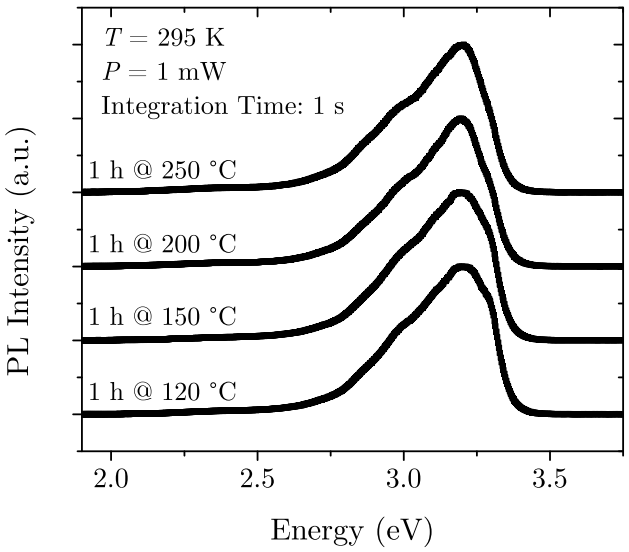


Figure 3.8: PL spectrum of the ZnO nanoparticles dispersion *ZN-3014A* from Nanophase Corporation Inc. under different temperatures (up to 250 °C) during the solvent vaporization step. No significant variation is observed as no sinter process takes place.

3.3 Gate Dielectric

The gate dielectric material is also a crucial component that significantly influences the transistor behavior as it is responsible for the capacitive coupling between the gate electrode and the active semiconductor. An effective coupling induces a higher charge carrier density at the transistor channel at a specific gate voltage. Conjointly, the gate dielectric layer must present low leakage current, low density of pinholes, and it must be reliable. Gate leakage currents in the order of $10^{-6} - 10^{-7}\,\mathrm{Acm}^{-2}$ are typically required for electronic circuits [CN15]. For these reasons, high-k materials are used as they have a higher effective capacitive coupling, which allows for a lower operation voltage and/or for a thicker gate dielectric film, reducing the leakage current and increasing the film reliability. Additionally to the electrical characteristics, the mechanical and chemical properties of the material are also important as they increase or restrict the integration process methods and the application field of the product. For instance, for the transparent and flexible electronic market, the gate dielectric should be transparent to the visible light spectrum, as well as endure the mechanical stress during both the fabrication process and the operation by the user. Further requirements are imposed by the substrate, which depicts low-temperature, mechanical and chemical stability; therefore, the dielectric deposition, curing step and operation must be compatible with these requisites.

A conventional gate dielectric used in the TFT technology is aluminum oxide deposited by ALD [FBM12, PMV+16]. On the one hand, the employment of such high quality dielectric with high relative permittivity is a good approach; on the other hand, ALD technique is a slow and cost-intensive process, and thick aluminum-oxide layers tend to break down when the flexible substrate is bent. Other high-k materials, such as hafnium oxide, hafnium lanthanum oxide and titanium oxide can also be used; however, these materials not only increase production costs, but their interface with the semiconductor is also worse comparatively to aluminum oxide, and they are even less compatible with the integration on flexible substrates [FBM12, PMV+16]. When using silicon wafer as back contact gate electrode, thermally grown silicon dioxide is largely employed. However, this approach is not an option for the integration on polymeric substrates. Additionally, low-temperature deposition of SiO_2 by PECVD leads to an instable dielectric layer [Hil14, Jae02]. Indeed, inorganic-based dielectrics present high relative permittivity, high dielectric strength and low leakage current, which makes them the primary option for the semiconductor industry. Conversely, their deposition requires cost-intensive vacuum processes or high annealing temperatures preventing their utilization on the low-cost sector and on flexible substrates.

Polymeric dielectrics, on the other hand, possess better characteristics when handling with flexible templates, as they are able to endure the mechanical stress suffered by the device during fabrication and operation [PMV+16, CN15]. These dielectrics, however, are reported to have lower dielectric constants [CN15]. Moreover, polymeric insulating materials commonly exhibit higher leakage currents and chemical instability [WS09, CN15], hence thicker layers are generally applied. In order to increase the capacitive coupling between the gate electrode and the active semiconductor, the employment of a hybrid system is a good approach. These systems combine the flexibility of the polymeric matrix and the high permittivity of inorganic compounds. As the integration of electronic circuits on flexible substrates is the main goal of this study, solution-based gate dielectrics compatible with the substrate characteristics were chosen. Based on the works of Diekmann [Die08] and of Wolff [Wol11], two groups of dielectric were used, one being a cross-linked polymer and the other a nanocomposite, which possesses a high-k character without decreasing the flexibility of the material.

3.3.1 Polymeric Dielectric

The most important characteristics of a polymeric compound to be employed in the TFT technology are its reliability and its performance, depicting low leakage currents, resistance to chemicals and minor degradation over time. For low gate leakage currents, the polymeric deposition must have high quality standards (pinholes free) and be robust. The operating voltage of the device can be lower if the dielectric permittivity of the compound is high or the polymeric layer is thin. Although the dielectric has to be resistant to the chemicals used in further fabrication steps; its structuration has to be possible in order to open via connections for the contacting of different conducting layers. One of the advantages of polymeric-based dielectrics is the usual deposition by solution-based processes. Therefore, similar techniques to the ones already described for the semiconducting layer can be employed. Taking into consideration the semiconductor, another important aspect is the interface between the insulator and the active channel region. This interface has to be smooth and has to possess low density of defects in order to avail a good charge carrier transport in the channel. Conjointly, the interface should exhibit adequate properties to facilitate the deposition of the subsequent material, which generally in bottom-gate setups is the active semiconducting compound. Commonly used organic dielectrics are polymers such as poly(4-vinylphenol) (PVP), poly(vinylalcohol) (PVA), polyimide (PI), poly(methylmethacrylate) (PMMA), polystyrene (PS), and poly(perfluorobutenylvinylether) (CYTOP) [WS09, CN15]. In order to reduce the thickness of the dielectric while minimizing pinholes, the polymer should be cross-linked forming a polymer chain. Additionally, this chain is commonly more resistant to the chemicals used in the TFT integration [WS09, CN15].

In this study, cross-linked PVP was used as gate dielectric in the integration of the TFTs. PVP is a weak acid polymer, and it is researched by several groups [VSS$^+$10, BMSS08, JDWM05, HLK$^+$06] due to its variety of applications and to its simple fabrication process. Besides its application as gate dielectric, this polymer is also used as responsive surface coating [UCEY10]. For the achievement of the cross-linked PVP, the polymer is normally dissolved in propylene glycol methyl ether acetate (PGMEA), whereas poly(melamine-co-formaldehyde)-methylated (PMCF-m) is used as a cross-linking agent [VSS$^+$10, CKM08, LKK$^+$07]. The proportion of 5:1:51 of PVP:PMCF-m:PGMEA, which is based on the study of Wolff [Wol11], was used in this work. Figure 3.9 presents the chemical structures of the polymer.

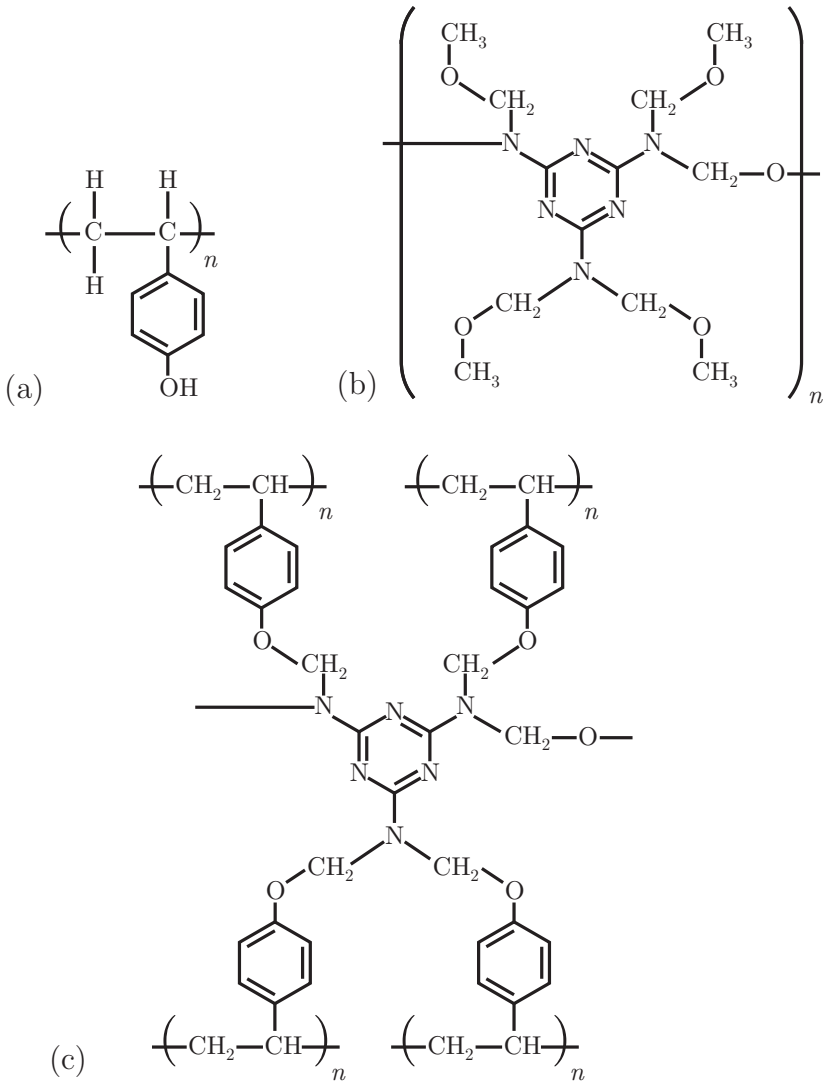


Figure 3.9: Chemical structures of the polymer used as gate dielectric. (a) Pure PVP, (b) cross-linking agent and (c) a cross-linked PVP chemical structure.

Through experimental measurements [Wol11], it was noted that the cross-linked PVP possesses a relative permittivity of about $k = 5.8$ for frequencies up to 10^5 Hz. As deposition method, spin-coating technique was used (low-spin phase = 800 rpm for 7 s; high-spin phase = 3000 rpm for 20 s). Subsequently, a pre-baking step on a hot-plate at 150 ℃ for 60 s for solvent vaporization and a further thermal treatment in a convection oven at 200 ℃ for 1 h to ensure the cross-linking reaction were performed in ambient air. A final dielectric thickness of about 180 nm was achieved. The structuration (via connections) was done by photolithographic technique and reactive ion etching (RIE) processing using oxygen as reactive gas, as described by [Wol11]. As the polymer is cross-linked, it endures the chemical stress caused by the solvents used in the photolithographic step.

The cross-linking reaction should not leave any mobile ions in the film, otherwise it may lead to instability effects in the transistor operation [VSS+10]. Due to a small variation in the amount of cross-linking agent in the PVP solution, an alteration in the adhesion of the aqueous ZnO dispersion used as active semiconductor to the polymeric film was observed. This effect was ascribed to the variation of the amount of hydroxyl (OH^-) groups at and in the cross-linked dielectric. Additionally, Lim *et al.* [LKK+07] and Faber *et al.* [FBJ+09] have reported that the use of PVP, especially due to the effect of OH^- groups in this polymer, leads to a shift in the turn-on voltage of transistors depending on the direction of the gate voltage sweep corresponding to a hysteretic behavior in the transfer characteristics. The presence of OH^- groups at the gate dielectric surface changes the PVP character from a nonpolar to a polar [LKK+07, VOLL04, JDWM05]. Moreover, polymer dielectrics, which contain a significant amount of hydroxyl groups inside or at the surface, are responsible for hysteresis in organic transistors as well as for a higher gate current leakage [KJJ+08, LKS+06, LKK+07].

3.3.2 Organic-Inorganic Nanocomposite

In order to increase the channel field-induced charge carriers at a specific gate voltage, the use of a high-k material should be considered. As discussed before, inorganic gate dielectrics, although possessing high permittivity, are cost-intensive (vacuum processing) and are not entirely suitable to flexible substrates, as the material layer commonly breaks down or defoliates when it is bent. Hybrid systems combining both the flexibility and solution processability of a polymeric matrix with the high coupling capacitance of inorganic compounds have been studied [CCH+04, FHTM15, BL07, CN15]. Concerning the

employment of inorganic-organic systems, there are different approaches, as for instance the application of bilayer or multilayers of materials [WAT+09, YJL+13, JWK+13], the incorporation of nanoparticles of an inorganic compound into a polymer [FHTM15, CN15] or the use of sol-gel processes [CN15].

In this study, a nanocomposite ($k = 12$ [DPH08]) was used as gate dielectric. This material purchased from Inomat GmbH (Neunkirchen, Germany) is based on hydrolyzed and condensed acrylate functionalized silane; soluble Ti components were introduced by co-condensation to adjust its permittivity (trade name: Inoflex [Ino15]). This high-k resin combines the advantages of the polymeric matrix (*e.g.* flexibility) and of the inorganic compound (*e.g.* high dielectric constant). The dielectric resin was diluted in 1:7 in 1-butanol and after its deposition by spin-coating process (low-spin phase = 800 rpm for 4 s; high-spin phase = 2000 rpm for 20 s) using a 0.45 μm PTFE syringe filter, it was cured and cross-linked by a thermal treatment (115 ℃ for 30 min in a convection oven in ambient atmosphere) and by an UV ($\lambda = 365$ nm and 200 $\mathrm{Wcm^{-2}}$) irradiation step (4 min of irradiation done in steps of 40 s exposure and 60 s of break to prevent excessive substrate heating). A final dielectric thickness of about $150 - 180$ nm was achieved. After being cured, the dielectric is stable against most of the solvents and chemicals used in the subsequent TFT integration steps.

For the structuration of the layer (via connections), photolithography technique and RIE process using fluoromethane (CH_3F) and argon (Ar), or wet etching using an alkaline solution containing sodium hydroxide (NaOH) were employed. However, in order to simplify its structuration, first experiments were performed taking advantage of the UV cross-linking step of the nanocomposite. Therefore, selected areas of the layer were partially exposed to the UV irradiation; the non-exposed areas could be removed using a solvent such as acetone or N-methyl-2-pyrrolidone (NMP), avoiding photolithographic and etching steps. Nevertheless, because of the design of the mask set available for the patterning of the TFT, these tests were discontinued.

Due to the sensitivity of the cured resin to alkaline solution, an overdeveloped photolithographic step on the dielectric may damage it, hence leading to instabilities in the transistor operation. This influence on the electrical performance of organic-based TFTs is described in [3]. Moreover, depending on the methods used during the drain and source structuration, the nanocomposite layer depicts a hydrophobic or a hydrophilic character. These properties can be used to improve the deposition quality of the next layer in the in-

tegration process of the TFTs. The influence of the surface character on the deposition of the water-based solution containing the ZnO nanoparticles is discussed in Section 3.6.1.

3.4 Contact Electrodes (Gate/Drain/Source)

The materials used for the electrodes are fundamental for the operation of the TFT as they are employed not only as active material for the gate, drain and source contacts, but also in the interconnection with adjacent components, as for instance, other TFTs, LEDs and capacitances. Metals and other conductors, as ITO (indium tin oxide), IZO (indium zinc oxide) and AZO (aluminum zinc oxide), can be applied depending on the system requirements.

For the gate contact, in which a low current flow (static operation) is usually observed in field-effect devices, the material is chosen primarily based on its compatibility with the integration process as well as on its reliability. Here, transparent materials as conductive metal oxides are also applied and researched in order to increase the field of application of the TFTs [WS09, CN15, PMV$^+$16]. Regarding reliability, gate electrodes integrated using sputtering technique usually possess a higher roughness compared to evaporated contacts, increasing, therefore, the instability of the deposited gate dielectric and its leakage currents [Wol11]. Another aspect that was experimentally analyzed was the impact of different methods used for gate electrode structuration [Pan06]. While etching processes leave a smooth surface for the deposition of the next layer, lift-off techniques create peaks at the borders of the structure originated by the non-conformal deposition of the gate electrode material. The intrinsic properties of the material itself, as the metal work function, are reported to have minor to none impact on the TFTs electrical characteristics. A direct comparison between chromium, titanium, copper and platinum has shown only minor variation in the electrical properties of GIZO-based TFTs [MPZ$^+$13]. However, when these materials are applied on flexible substrates, mechanical properties as the Young's modules are important, since they define if an irreversible mechanical deformation of the template will or will not occur. This outcome is described in the next section, in which flexible substrates are explored.

The choice of the drain and source electrode material is, on the other hand, crucial for the operation of the transistor. The material is in direct contact with the active semiconductor; hence it is partially responsible for the charge carrier flow through the

TFT. In this study, metals were chosen for the integration of the electrodes, mainly due to their high conductivity (lower resistance in comparison to metal oxides) and to their availability and prior knowledge in situ regarding their structuration and characteristics. The selection of the metal was based on the work performed by Wolff [Wol11], in which different materials were evaluated as contacts focusing on the electrical characteristics of the device. Since ZnO was employed as active semiconductor, aluminum was the logical choice for the drain and source electrodes as, between the tested materials [Wol11], it has depicted the best performance.

Even though gold is also a promising alternative to be employed as drain and source material, it has shown some issues regarding leakage currents in the transistor off-state regime, which was ascribed as an ambipolar conduction of the semiconductor [Wol11]. An advantage of gold is the possibility to deposit it by a printing process of a dispersion containing nanoparticles of this material. Due to the use of nanoparticles, the sinter process to form a film can be done at temperatures as low as 140 ℃, and the final layer possesses characteristics similar to vacuum-deposited films [WLO$^+$05]. Silver can also be deposited and structured through solution-based techniques [HJL$^+$16, MNL$^+$14, SIK$^+$14]. Hence, Ag contacts can also be applied as gate, drain and source [DK07, SIK$^+$14, HJL$^+$16]. First experiments using evaporated silver as gate electrode metallization have shown some issues regarding its oxidation and local film roughness, inducing higher leakage currents and break down of transistors, as shown in Section 5.2.

3.5 Substrate

The TFT technology has already been investigated for decades which enables its employment in a wide range of new applications and products. Along with the fact that its integration process is almost independent of the substrate (generally used just as mechanical support), there is the possibility to explore also the mechanical and optical properties of the applied materials. As a consequence, this technology is in ascendency, and it has the potential to be constantly present in our daily lives in the upcoming years.

To accomplish this goal, the characteristics of the substrate are as important as the entire integration process. Although this mechanical support has minor influence on the TFT performance, when employing flexible substrates, several adaptations to the integration process are required. Most of them are related to the fact that such substrates

can only be handled at limited temperatures, to their sensitivity to chemicals or to their flexibility, *i.e.* all deposited materials suffer from mechanical stress during the device fabrication or use. For instance, the use of non-malleable metal connections or dielectrics may induce damages after bending the template. For this sake, all components (materials and integration processes) have to be carefully selected to be compatible with the substrate. There are different groups of materials that can be used as template in the fabrication of flexible electronics. Metal substrates, such as aluminum or stainless steel, were already tested primarily due to their capability to endure high temperatures [KKJRH10, MMH+14]. The main drawback of these materials, however, is their conductivity, requiring an insulating layer on top of the substrate, increasing the device's weight and production costs. Additionally, the application of such layer on a metal produces parasitic capacitances and cross-talk effects in the transistor operation. Nowadays, aiming to better production cost and biological application, paper and other biodegradable materials are being also researched as an alternative for TFT templates [PMV+16]. Nonetheless, there are still concerns related to their instability and durability.

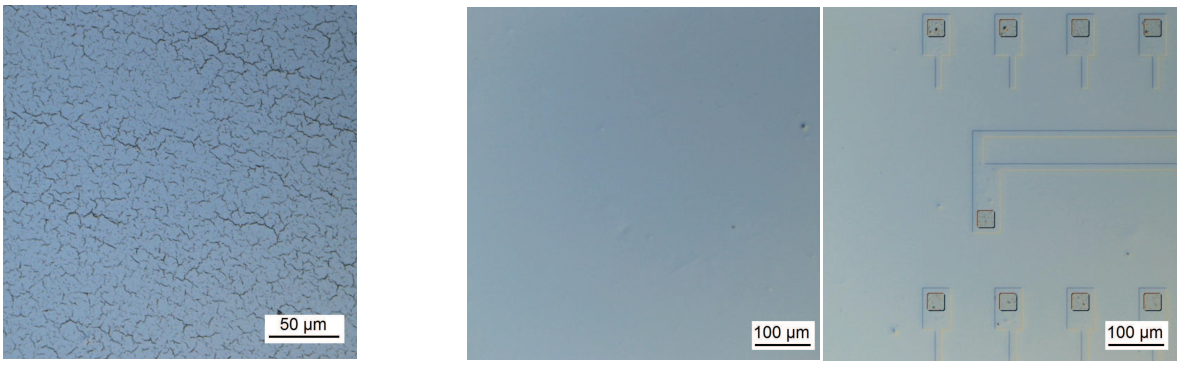
In this study, the materials used as substrates are polymers due to their properties and availability. Besides their flexibility, polymeric templates are commonly transparent to the visible light spectrum, which increases the field of applications of the devices integrated on them. Generally used polymers are: polyimide (PI)[8], polyethylene terephthalate (PET), polyethylene naphthalate (PEN), polyether ether ketone (PEEK), polycarbonate (PC), polypropylene (PP), polysulfone (PES), polyvinyl chloride (PVC), polyvinyl alcohol (PVA), parylene, and polydimethylsiloxane (PDMS). Each polymer has advantages and disadvantages related either to the applications or to the integration process. For instance, PI has attracted attention because of its high-temperature stability and surface quality; however, due to its yellowish to brownish color, its applications for transparent electronics are limited. Another example is the use of PDMS, which is highly stretchable and biocompatible; conversely, its processing and handling with standard techniques are complex [WS09, CN15, PMV+16]. PVC and PET were the primary investigated substrates here. PVC foils have shown insufficient chemical stability, being damaged by common photolithographic solvents. Additionally, further instabilities related to thermal deformation appeared when the substrate was heated to 115 ℃ during the curing of the photoresist.

[8] Polyimide (PI) is commercially known as Kapton®.

Based on their chemical and thermal stability, PET substrates were chosen and used for the integration of the TFTs. First experiments were performed on a CG3700 substrate from 3M [3M97]. The foil, however, was designed to be used for laser printing machines, thus it was coated with a layer to improve the toner adhesion. The coating layer was not stable against the solvents, such as acetone and isopropanol, used in the integration process. Therefore, this layer was removed in an ultra-sonic bath in acetone followed by a cleaning procedure with isopropanol. As discussed by Diekmann [Die08], the density of local deformities originated during the substrate fabrication process induces a reduction in the operation voltage of the transistors due to dielectric breakdown. After the coating removal, the PET foil showed a high density of these defects disturbing the structuration of the subsequent layers. Moreover, residual flakes of the insoluble part of the coating layer were usually observed, increasing even more the number of defects on the substrate. To reduce the effects of the already existent defects on the template, the application of a barrier layer was performed. Therefore, a layer of the nanocomposite (the same employed as gate dielectric) was applied; however, besides the increase in the complexity of the integration process and in costs, this extra step in the fabrication was responsible for introducing additional instabilities in the definition of the gate electrode and in the subsequent photolithographic processes. At this point, two approaches were considered: one related to the improvement of the barrier layer and the other related to the choice of the primary PET substrate. The second route was chosen aiming to maintain the integration as simple as possible, and to avoid any additional step.

As a result, a cooperation with Mitsubishi Polyester Film GmbH was established. Based on the requirements demanded by the TFTs integration process, the Hostaphan® GN biaxially oriented PET series was indicated as the substrate with the best features. This series is characterized by high transparency, smooth surface (low defect density), excellent mechanical strength and dimensional stability. As a tradeoff between the stability during the handle of the substrate and its flexibility, a 75-μm thick substrate was selected. The main characteristics of the PET foil are: 91 % transparency in the visible light spectrum; Young's modulus from 4000 $\mathrm{Nmm^{-2}}$ to 4800 $\mathrm{Nmm^{-2}}$; roughness average (R_a) of 10 nm; and shrinkage of less than 1 % at 150 °C. Further information regarding the substrate can be found in the product datasheet [Mit16].

Specifically related to the integration process applied in this study, the substrate is resistant against the employed chemicals as well as to the used temperature range. The template is malleable enough and lined up with the mechanical requirements for later flexi-



(a) (b)

Figure 3.10: Metallization on 75-μm PET foils using (a) 50 nm chromium and (b) 50 nm aluminum and a second metallization of 150 nm aluminum on top of a partially structured template.

ble electronics integration. The physical deformation caused by the temperature gradients, by the mechanical load, and by supporting the TFT structures are of minor influence in the integration process. Conjointly, as the substrate was acquired through a cooperation with Mitsubishi Polyester Film GmbH, it is available in diverse sizes, and it is suitable for mass production at low costs.

The compatibility of the Young's modulus of the chosen compounds and substrate used in the TFT fabrication is also a concern and should be addressed. For instance, when chromium, that depicts a high Young's modulus (around 279000 Nmm^{-2} [SBB92]), is used as metallization layer, an irreversible bending of the substrate occurs if the ratio between the substrate and the metal thickness is low. Additionally, due to the low elasticity of chromium, cracks in the metallization can be observed, as shown in Figure 3.10a. These cracks disable a reliable current flow through the metal layers being unappropriated for electronic circuits fabrication. For this sake, the material selection is an important aspect in the integration process of devices on polymeric substrates.

Metals with lower Young's modules, such as aluminum (around 70000 Nmm^{-2} [SBB92]) and gold (around 79000 Nmm^{-2} [SBB92]), are more compatible with the integration process on flexible templates. For the TFTs integrated in this study, aluminum evaporated under high-vacuum conditions was applied as the main metallization layer. Besides the matching of the electrical characteristics when in contact with ZnO, this metal was used due to its mechanical and chemical properties, which allow an adequate etching process and are compatible with the further integration steps, as described in the upcoming Section. Figure 3.10b depicts a single aluminum metallization (note the absence of cracks

and defects), as well as a second aluminum metallization on a partially structured template (with gate electrodes and via connections through the gate dielectric) showing the compatibility of this material with the TFT integration process. In order to avoid initial influence of the flexibility of the polymeric substrate, the integration process and electrical characterization of the TFTs were firstly performed on rigid substrates. Therefore, oxidized silicon[9] and borosilicate glass[10] wafer were employed.

3.6 Processing

The structuration of the layers on flexible substrates is, in general, similar to the one on rigid substrates. Techniques such as etching and lift-off are often used. However, due to the chemical, mechanical and thermal sensitivity of the polymeric substrates, some adaptations are required. The employment of shadow masks is used by several research groups; by applying this simple integration process, most of the chemical stresses, that the substrate and previous deposited layers must endure during the photolithography, etching and lift-off processes, are avoided. Conversely, the use of shadow masks limits the structure resolution to around 10 μm or even larger, depending on the deposition method and on the mask density. Through a complicated and time intensive employment of a set of shadow masks, alignment systems and deposition methods, higher resolutions were also reported [AKZ$^+$12, ZRL$^+$13]. However, further issues related to the layer reliability and to the mask fixing system are faced when large area substrates are used. Moreover, shadow mask technique is not entirely suitable for large-scale production of compact and energy-efficient electronic circuits.

The mechanical stress suffered by the template is commonly dodged by fixing the polymeric foil on a rigid substrate, as a silicon or glass wafer. This technique, however, does not make use of the substrate flexibility and masks possible defects originated from the mechanical stress during the device fabrication. A damage-free release of the flexible substrate is complicated and requires extra processing steps increasing production costs. For this reason, devices are generally electrically characterized without removing it from the rigid mechanical support. In case of an integration process without this support, such practice can lead to an unexpected variation of the transistor's electrical characteristics.

[9] Standard 100 mm Si-wafer with more than 300 nm thermally grown oxide.
[10] Borosilicate glass wafers with 100 mm cross-section and 0.5 mm thickness from Plan Optic AG.

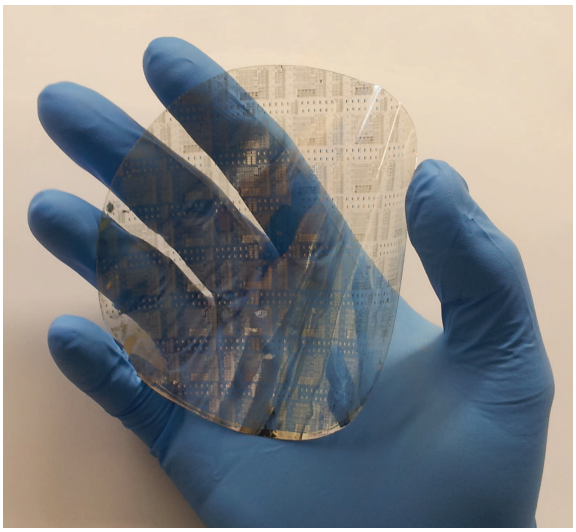


Figure 3.11: Image of the PET substrate with the integrated TFTs.

In this study, first experiments were performed by fixing the polymeric substrate to a Si wafer. Alternatively from the approach used by Diekmann [Die08], in which an irreversible fixing method was applied, a PI-based tape was employed. Several substrate shapes and sizes were tested, varying from square and polygonal shapes to round ones, and from over-dimensioned to same-sized and under-dimensioned regarding the rigid mechanical support size. Notwithstanding, it was evidenced that the fixing step was extremely time consuming and not compatible with the machinery and processes used during the integration. More than that, the resolution and yield achieved in the photolithography were unsuitable.

An alternative and promising method investigated to avoid these issues is the use of freestanding flexible substrates. Moreover, this procedure avails a more realistic scenario of the mechanical stress suffered by the elements during a later large-scale production. Nonetheless, during the contact photolithographic process and dielectric deposition, the substrate has no support and its handle is complicated. As a solution, the PET foil is only temporary fixed by a vacuum system during these fabrication steps[11]. This temporary fixing enables an adequate photolithographic process on the entire substrate, as depicted in Figure 3.11. A 100-mm silicon wafer was used as model for the shape and size of the flexible template, because the available photomask set and machinery were already designed and adjusted for this dimension.

[11] The development of the fixing system and the adaptation of the photolithographic technique on flexible substrate was performed in cooperation with Thorsten Meyers at the Paderborn University. The process was published in [5].

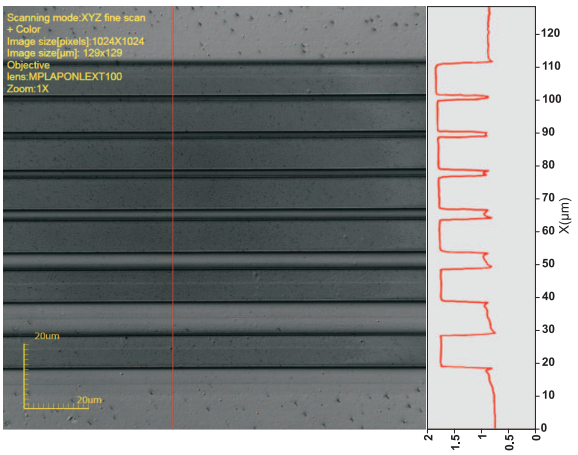


Figure 3.12: Confocal laser microscope image of a photolithography process on a 75-μm thick freestanding PET substrate after the metallization.

Another important aspect of the developed process is the quality of the resolution of the photolithography technique on the PET substrate. The result of the process was analyzed using an Olympus LEXT 3D Measuring Laser Microscope OLS4000. Figure 3.12 depicts the quality of the photolithography with a resolution of about 1 μm for the definition of the drain and source electrodes prior to the etching of the aluminum layer. As a consequence of the temporary vacuum fixing system, it is possible to align different masks sustaining the definition of multiple layers on a freestanding flexible substrate without deteriorating the resolution.

3.6.1 Device Integration Procedure

Based on the improved contact quality between the active semiconductor and the drain/ source electrodes of inverted staggered setups, the nanoparticle-based TFTs were firstly evaluated applying this design. The general procedure for inverted staggered structures is depicted in Figure 3.13. Lined up with the work performed by Wolff [Wol11], the following processing was employed on oxidized silicon wafer using PVP as gate dielectric.

A standard 100-mm silicon wafer was used for the integration of the ZnO nanoparticle TFTs. Since the silicon wafer was used just as mechanical support, the wafer was thermally oxidized in order to achieve a 300-nm oxide to insulate the bulk silicon from the transistors. Afterwards, a 50-nm thick aluminum layer was evaporated under vacuum conditions and structured by photolithographic and wet-etching processes to integrate the gate electrodes. The aluminum etching solution contains 80 % of phosphoric acid

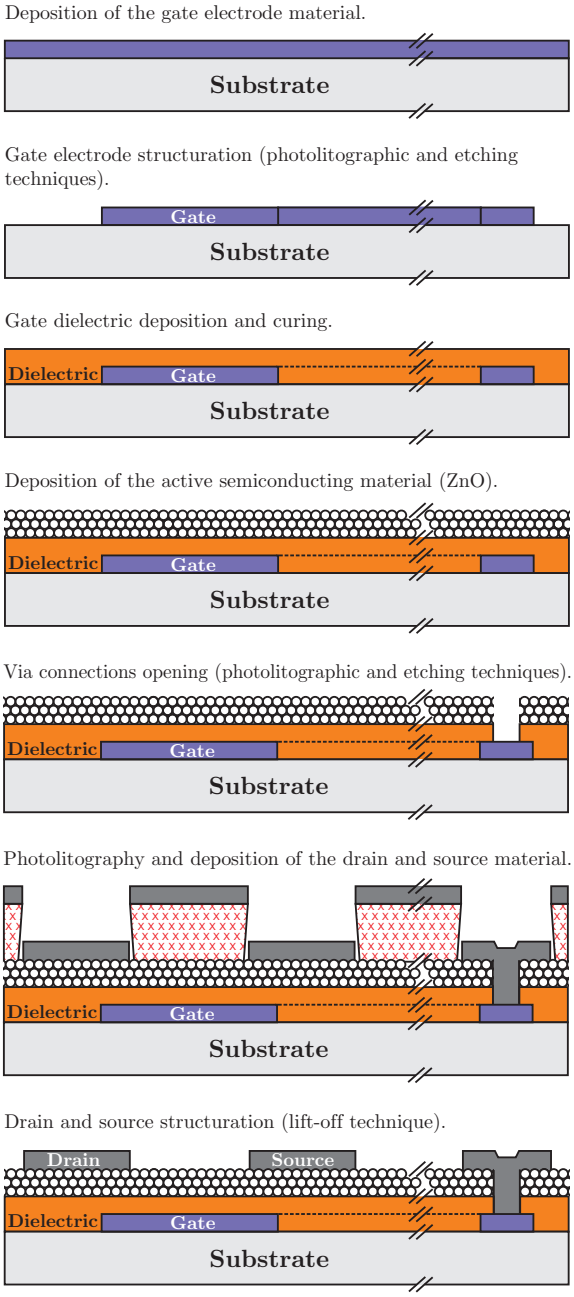


Figure 3.13: General integration process of inverted staggered TFTs employing ZnO nanoparticles as active semiconductor.

(H_3PO_4), 5 % of acetic acid (CH_3-COOH), 5 % of nitric acid (HNO_3) and 10 % water giving an etching rate of about 15 nm/min at room temperature[12]. For the gate dielectric layer, 180 nm of PVP was spin-coated on the sample. An ultrasonic agitation was performed on the aqueous dispersion of gas phased synthesized ZnO nanoparticles provided by Degussa GmbH in order to break down the agglomerations of nanoparticles. Thereafter, the solution (2 ml) was deposited by spin-coating process at 3000 rpm for 30 s. To fasten the nanoparticles to the surface and to ensure a full removal of water, a soft bake at 110 ℃ for 5 min followed by a hard bake for 1 h at 200 ℃ in ambient air were performed forming a layer of about 300 nm thickness. Via connections were opened through the semiconductor and gate dielectric using photolithography and a wet-etching step in an aqueous solution of ammonium fluoride (NH_4F), acetic acid (CH_3-COOH) and propylene glycol, and reactive ion etching with oxygen (O_2) to etch the ZnO nanoparticles and the gate dielectric layer, respectively. Afterwards, aluminum (150 nm) was deposited by evaporation and structured (drain and source electrodes) by lift-off technique.

Due to the unstable transistor operation, investigated and discussed in Section 4.2, and to the high temperature required for the PVP cross-linking reaction, which partially prevents its utilization on a wide range of polymeric substrates, the integration process was adapted to employ the high-k nanocomposite resin as gate dielectric. After the gate electrode structuration and before the gate dielectric deposition, the wafer surface was treated in a 500 W oxygen plasma for 4 min to remove organic contaminations and to improve the surface wetting properties. Then, the spin-on high-k resin was deposited and cured/cross-linked by the combination of thermal treatment at 115 ℃ and UV irradiation forming an about 200-nm thick (due to the activation in oxygen plasma) gate dielectric layer. Afterwards, a 20 s oxygen plasma treatment was performed to activate the surface of the dielectric layer for the ZnO nanoparticles deposition. The via opening through the semiconductor and through the gate dielectric was performed using photolithography and wet chemistry (aqueous solution of ammonium fluoride (NH_4F), acetic acid (CH_3-COOH) and propylene glycol), and reactive ion etching with fluoromethane (CH_3F) and argon to etch the ZnO nanoparticle and the gate dielectric layer, respectively. Drain and source electrodes were fabricated by a subsequent evaporation of a 150-nm thick layer of aluminum using lift-off technique.

[12] The etching processes were preferably conducted at room temperature. This was done aiming at a better and smoother later transfer of the process to polymeric substrates.

As described in Section 4.2, along with the reduction of the TFT operating voltages and the increase in the transistor stability and performance by employment of the high-k nanocomposite, a hysteretic behavior in the transistor's I-V curve was still observed. This instability effect can be ascribed either to the chemical and physical stress suffered by the semiconductor during the drain/source structuration or to the high density of defects observed in the ZnO nanoparticles. Therefore, inverted coplanar TFTs were integrated to identify the origin of the instability, albeit the lower quality of the contact between the drain/source electrodes and the semiconductor. During the investigation employing the inverted coplanar setup, different dispersions containing ZnO nanoparticles (already listed) and precursors were evaluated. The main results concerning the electrical characteristics of the precursor-based TFTs are described in Section 4.1 and the ones regarding the TFTs with the nanoparticle dispersion in Section 4.2.

Additionally to the transistor setup modification, the integration process was improved to be compatible to the polymeric substrate. The main changes are related to the methods used for the via connections structuration, to the maximum process temperature and to the absence of O_2 plasma treatment for the activation of the dielectric layer prior to the nanoparticles deposition. Previously, the etching of the high-k resin was done employing a reactive ion etching system; however, this process is not fullly compatible to the polymeric substrate. Therefore, the nanocomposite etching process was performed applying an alkaline solution based on NaOH. This etching process depicts good selectivity to the unexposed photoresist part, even considering the isotropic character of the development process and dark erosion. Because of the sensitivity of the aluminum gate electrode to the solution, a protective layer of 7 nm titanium was evaporated on the wafer prior to its structuration. Conjointly, the maximum temperature was defined to be 115 ℃ when the positive aspect of the photoresist[13] was used, while it was defined to be 120 ℃ when the reverse bake process was used (generally, if lift-off technique is applied). The structures were pre-defined by the available photomask set.

The general procedure for inverted coplanar structures is depicted in Figure 3.14. An oxidized silicon wafer was primary used and only processes that are fully compatible to flexible substrates were performed. Subsequently to the deposition of the layer sequence of 50 nm aluminum and 7 nm titanium under high-vacuum conditions, the gate electrodes were formed by a contact photolithography technique followed by wet-etching processes.

[13] The photoresist Clariant AZ 5214E can be employed using its positive or negative tone character depending on the processing performed as described in [Mic00].

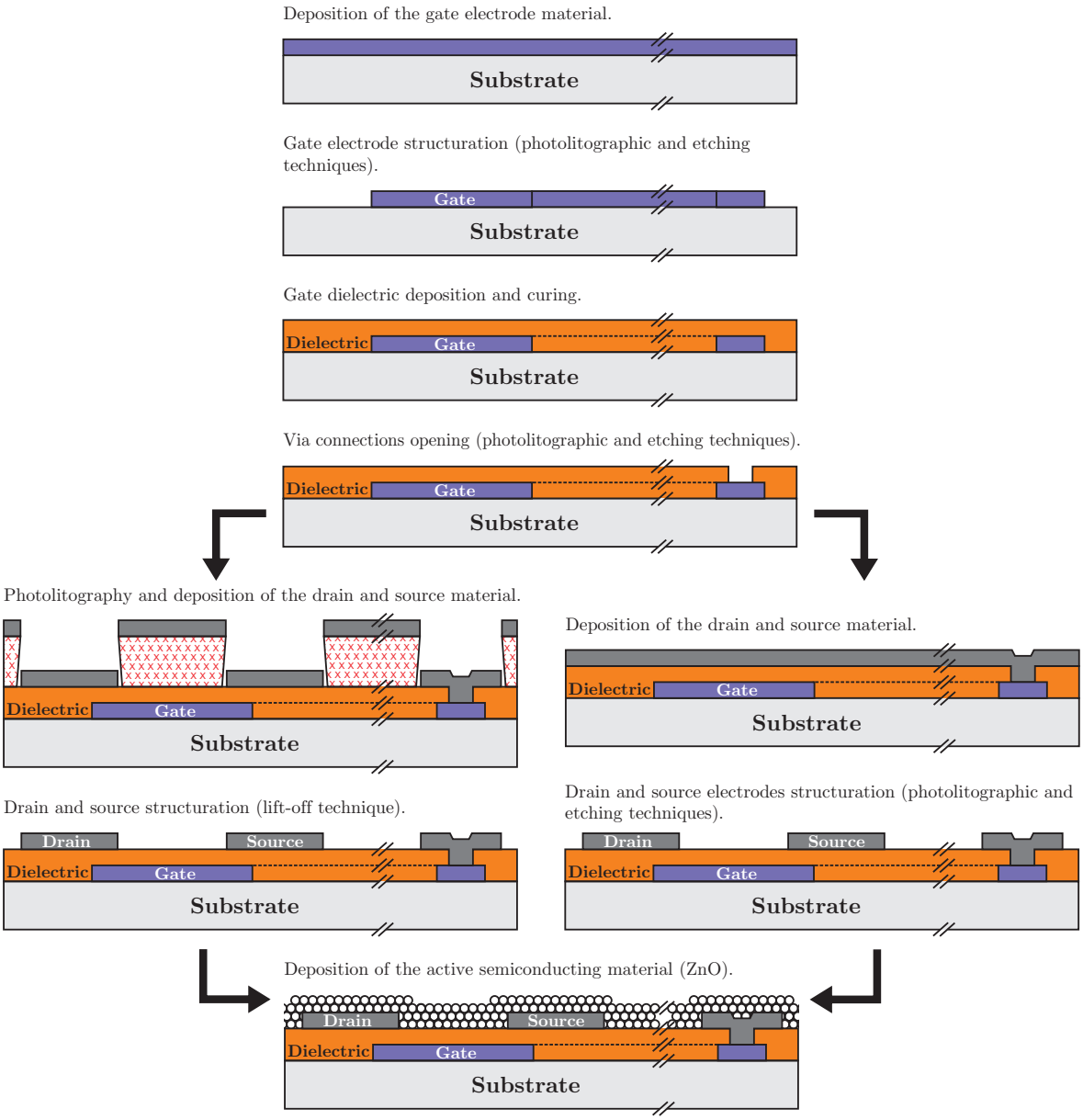


Figure 3.14: General integration process of inverted coplanar TFTs employing ZnO nanoparticles as active semiconductor.

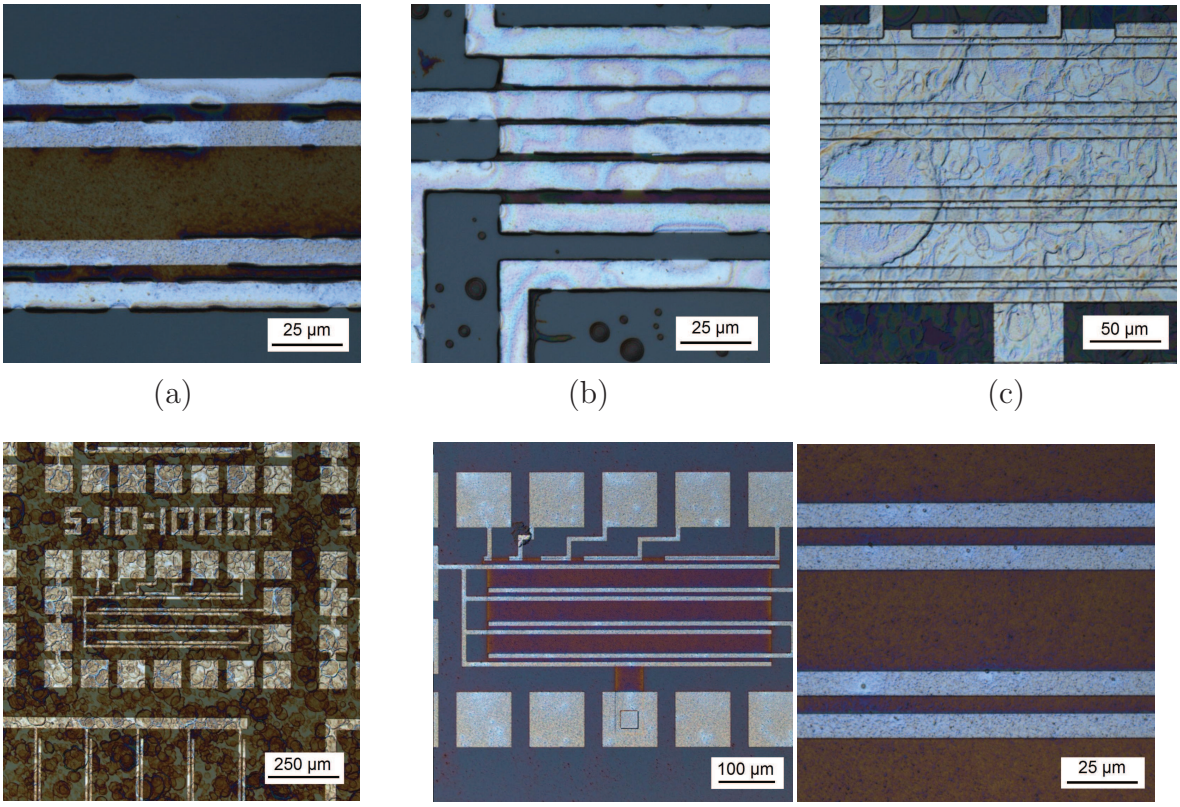
The titanium layer was etched at room temperature using an aqueous solution containing ammonium hydroxide (NH_4OH) and hydrogen peroxide (H_2O_2). The etching of aluminum was performed as previously described for the inverted staggered setup. Then, the spin-on high-k resin was deposited and cured/cross-linked forming a 150-to-180-nm thick layer. Via contacts were opened through the gate dielectric using photolithographic process and wet chemistry technique.

The next step is the structuration of the drain and source contacts that is followed by the deposition of the semiconducting layer. Due to the attractive properties of the water-based dispersion containing the ZnO nanoparticles, the main discussion here concerns its processing and deposition, whereas the results on the TFT electrical characteristics are discussed in Section 4.2.

After the gate dielectric patterning (via connection opening), the drain and source contacts were integrated by photolithography and lift-off techniques of a 150-nm thick aluminum layer evaporated under high-vacuum conditions. After this processing, the gate dielectric exhibits hydrophobic character. By using a spin-coating process for the deposition of the ZnO water-based dispersion without O_2 plasma, the adhesion between the nanoparticle dispersion and the gate dielectric is deficient[14]. Figure 3.15a depicts the uneven deposition of the nanoparticles, which results in poor transistor's electrical performance and low yield. The use of spray-coating has some advantages based on the absence of centrifugal forces (present in spin-coating processes) and on its better compatibility to large area substrates. Due to capillary effect, the main portion of the nanoparticle dispersion fills the active transistor channel area (see Figure 3.15b) increasing transistor yield and performance. Notwithstanding, the difference in the surface energy of the aluminum (drain and source electrodes) and of the gate dielectric induces agglomeration of the dispersion on the metal contacts.

In order to improve the active semiconductor deposition, the spray-coating technique was applied on a 60 ℃ heated substrate. The simultaneous solvent evaporation and deposition of the nanoparticle solution lead to the formation of a nanoparticulated film. Despite the improvements in transistor yield and in the uniformity of the deposition, this approach induces the formation of large grain boundaries (Figure 3.15c) and trapping of charge carriers in the semiconducting film. Another approach to improve the deposition

[14] The results concerning the quality of the deposition of the water-based ZnO nanoparticle dispersion were partially published in [16].



(a) (b) (c)

(d) (e)

Figure 3.15: Nanoparticle depositions using different surface treatments and deposition techniques; (a) spin-coating, (b) spray-coating and (c) spray-coating onto a heated template on hydrophobic surfaces, (d) spray-coating on O_2 plasma treated surface, and (e) spin-coating on hydrophilic surface.

of a water-based solution on the template is to enhance the wetting property of the gate dielectric. A hydrophilic surface can be achieved by an O_2 plasma treatment. After the samples were treated for 20 s in a 500 W O_2 plasma, the semiconducting dispersion was applied, the result is shown in Figure 3.15d. On the one hand, the improved deposition of the ZnO nanoparticles increases the number of operating devices. On the other hand, during the O_2 plasma step, the drain and source Al-based electrodes are oxidized decreasing the contact quality to the ZnO and, thus, the current level in the transistor. Additionally, due to the presence of energetic ions in the plasma, the gate dielectric is also damaged, increasing leakage currents and instability effects.

It was noted that, if the drain and source electrodes are integrated using a wet-etching process instead of a lift-off technique, the gate dielectric layer exhibits a hydrophilic character[15]. In this case, by depositing the nanoparticle dispersion by a spin-coating process, the semiconducting material is able to cover most of the sample (Figure 3.15e). Nevertheless, the already structured drain and source electrodes and the centrifugal forces caused by the spin-coating process lead to an uneven deposition of the nanoparticles, which decreases the quality of both the internanoparticle connections and the contacts between the drain and source electrodes. Based on previous results achieved using spray-coating, the nanoparticles were deposited by this technique on the hydrophilic surface after the definition of the drain and source electrodes. Due to the good substrate covering and to the improved transistor performance, this method was selected for the inverted-coplanar-device integration on flexible substrates, as shown in Figure 3.16.

In Figure 3.16, it is also possible to observe that the integration process is fully compatible with the PET substrate. Along with the high resolution achieved in the photolithography on flexible substrates, another important aspect to be highlighted is that the material of the drain and source electrodes can be changed. This flexibility in the template fabrication avails the same process to different semiconductors. The choice of the material for a specific semiconductor will depend on the position of its work function with respect to the valence/conduction band of the inorganic semiconductor or to the frontier molecular orbitals (highest occupied molecular orbital, HOMO, and the lowest unoccupied molecular orbital, LUMO) if an organic semiconductor is used. For example, the employment of gold for the drain and source electrodes on the template enables the evaluation of organic

[15] The high-k nanocomposite surface character modification from hydrophobic to hydrophilic is ascribed to the variation on the surface roughness and on the amount of OH^- present at the surface. The origin of such effects are still under research and more information can be found in [3].

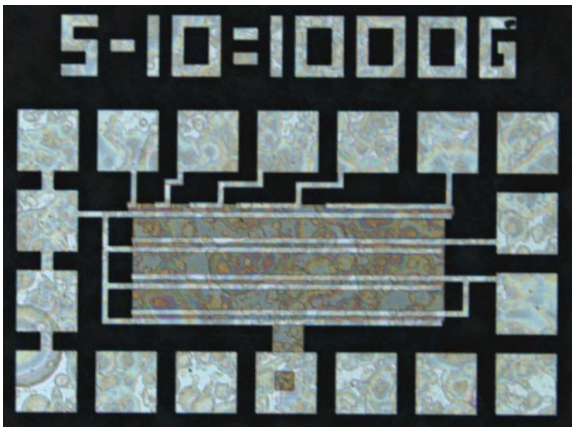


Figure 3.16: ZnO nanoparticle TFTs set integrated on PET substrate using a spray-coating process on a hydrophilic surface.

semiconductors such as pentacene or DNTT [Sir14, WS09]. Nevertheless, the use of other materials for the electrodes (source, drain and gate) and interconnections will also depend on the Young's modules of the chosen materials, as already discussed. For this reason, the range of possible compounds is limited, at least for certain thicknesses.

Following the integration procedure, the semiconductor is usually the next to be deposited. Depending on the properties of the compound and on the deposition method, the characteristics of the gate dielectric surface also play an important role in the deposition quality. For example, if a water-based solution is used, the hydrophilic surface achieved by the etching process will lead to a formation of a reliable layer. Conversely, the hydrophobic surface character after the drain and source electrodes structuration by lift-off technique induces a better deposition quality when other solvents are used. For inorganic semiconductors deposited by vacuum techniques, such as sputtered ZnO, the surface properties of the gate dielectric will not directly influence the deposition quality; although the roughness at the interface leads to charge carrier trapping. Nevertheless, the surface energy may induce a shift on the electrical characteristics of the transistors or, in case of organic semiconductors, a different crystalline growth. A deeper work concerning its influence on the characteristics of the organic semiconductors DNTT and C_8-BTBT can be found in [2] and [3].

The active semiconductor was selected based on its handling, solution stability, deposition quality, and electrical performance (TFT characterization) using an inverted coplanar setup. Additionally, the stabilization of the ZnO nanoparticles by UV irradiation and wet-air treatment (described in Section 4.2) was also performed in this setup. Afterwards, the

device structure was again transferred to an inverted staggered design due to the better performance usually observed in such setups.

For the inverted staggered setup, the processes up to the gate dielectric deposition and curing/cross-linking step are the same as the ones followed for the inverted coplanar setup. After the deposition of the nanoparticulated dispersion by spin-coating technique, via connections through the semiconducting layer and through the gate dielectric were opened to contact the gate electrode. The drain and source electrodes were structured by lift-off technique of a 150-nm thick aluminum layer evaporated under high-vacuum conditions. During the transfer process to the inverted staggered setup, some adaptations regarding the deposition of the semiconducting layer and the stabilization of the nanoparticle were done. These adjustments as well as the transfer of inverter staggered structures to PET substrates are described in Section 4.3.

CHAPTER 4

ZINC OXIDE TRANSISTORS

The ZnO transistors integrated according to the processes described in Chapter 3 were electrically characterized following the method addressed in Section 2.2.4. This chapter focuses on the characterization analysis and performance evaluation of the TFTs. The first part of the discussion is related to precursor-based TFTs, especially the ones associated to the nitrate-based semiconductor. Nonetheless, due to the intensive research in nanoparticulated ZnO films, the main part of this study is focused on the analysis of nanoparticle-based devices. First, the transport mechanism of charge carriers through the nanoparticulated film and its effects in the TFT behavior are presented. The second subsection is related to the identification and reduction of the instabilities in the transistor operation performed on rigid substrates. Afterward, the transfer of the integration process to flexible substrates is discussed. Finally, the transistor performance improvement by the application of an inverted staggered setup on rigid as well as on flexible substrates is presented.

4.1 TFTs with ZnO Precursors

The application of precursors is widely used for the integration of metal-oxide transistors [DJS+15, KYK14, FBM12, PMV+16]. As discussed in the previous chapter, the use of different precursors (chlorine-, acetate- or nitrate-based) leads to an adaptation of the integration processes as well as different temperature requirements for materials synthesis

[KYK14]. In order to keep this temperature as low as possible, acetate- and nitrate-based ZnO precursors were evaluated.

The first experiments employing the zinc-acetate-based precursor were performed on a p-type Si wafer using about 200 nm of thermally grown SiO_2 as gate dielectric to simplify the fabrication process of the template and the evaluation of the electrical characteristics of the transistors. In order to increase the contact quality between the gate electrode (Si wafer) and the measurement system, the oxide on the wafer's backside was removed; aluminum (> 200 nm) was then evaporated under high-vacuum conditions and annealed at around 400 ℃ for more than 30 min to ensure a low-resistance contact to the Si. The drain and source electrodes (150 nm of e-beam evaporated aluminum) were structured by photolithography and wet-etching techniques. As described previously, the acetate-based precursor was maintained at a temperature of 60 ℃ prior to its deposition on the transistor template. As a result of the temperature difference between the wafer and the precursor, as well as of the temperature variation when the solution was transferred to a syringe, the deposition quality on the wafer was deficient. This accounted for a high density of defects; cracks and irregularities on the film. Aiming at the enhancement of its wetting properties, the template was pre-treated in O_2 plasma; however, the film formation was still not reliable, preventing the use of this precursor to achieve ZnO as an active semiconducting material. Under these circumstances, attempts to improve this deposition method as well as to produce operating transistors using this process were halted. Nevertheless, an interesting effect was observed when this water-based precursor was deposited on top of the nanoparticulated ZnO film. In this case, an improvement in the TFT electrical characteristics and a reduction of the hysteresis in the transistors transfer curves were noted, as discussed in Section 4.2.

The employment of the nitrate-based precursor in the integration process depicted more promising results than the acetate precursor variation; a semiconducting film was easily deposited onto the transistor template. ZnO TFTs were integrated in both inverted coplanar and inverted staggered structures using ammine-hydroxo zinc precursor applying temperatures below 150 ℃. The precursor preparation, presented in Section 3.2.2, was based on the work of Meyers *et al.* [MAH+08], in which a chemical procedure for a nitrate-based precursor was proposed, allowing the formation of a polycrystalline ZnO layer with simple processing steps and with limited synthesis temperature.

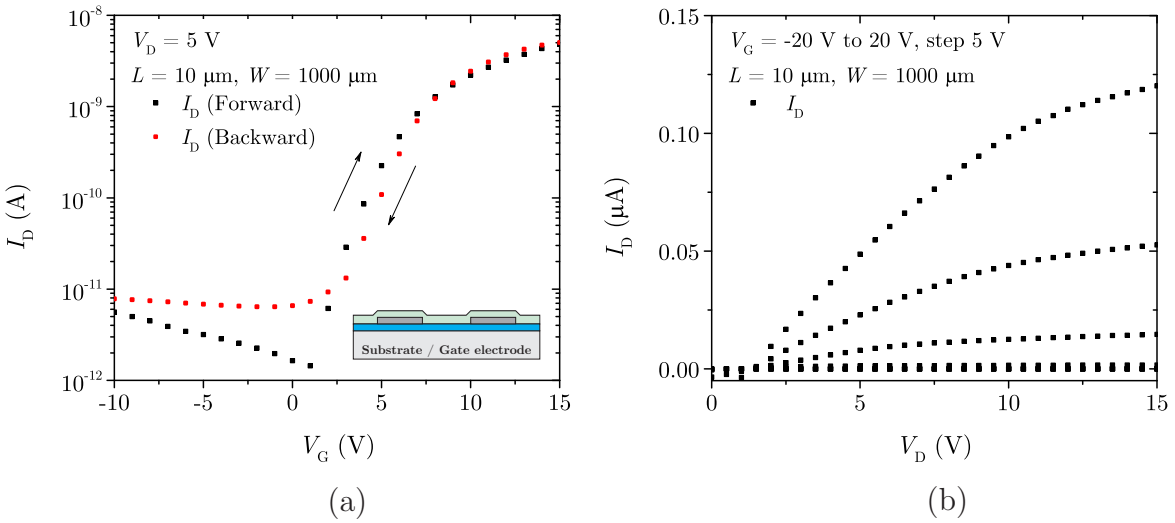


Figure 4.1: Input (a) and output (b) characteristics of a ZnO TFT with the deposition of one layer of the nitrate-based precursor integrated in an inverted coplanar setup. The inset depicts the cross-section of the TFT.

For the inverted coplanar structures, Si wafer, SiO_2 and Al were employed as gate electrode, dielectric, and drain and source electrodes, respectively, applying the same process used for the TFT with the acetate-based precursor. After the deposition and thermal treatment of the amine-hydroxo zinc, the transistors were electrically characterized. The input and output characteristics of the ZnO TFTs with inverted coplanar structure are depicted in Figure 4.1. The transfer characteristic exhibits minimal hysteresis. The transistor V_{ON} is approximately 2 V and the V_T is around 3.4 V, extracted from the linear extrapolation of the $I_D^{1/2}$ graph. The field-effect mobility, extracted from the transconductance, is $8 \cdot 10^{-5}\,cm^2V^{-1}s^{-1}$, the I_{ON}/I_{OFF} ratio is about 10^3 and the subthreshold swing is 2.1 V/dec.

As already addressed, for inverted coplanar setups the main limitation of the transistor performance is the quality of the contact between the semiconducting layer and the drain and source electrodes. Additionally, due to its ammonia content, the nitrate-based precursor interacts with the aluminum electrodes, increasing the instability of these contacts. These issues can be avoided through an inverted staggered setup, in which the metal electrodes are placed on top of the semiconductor following its irregularities. For the integration of such setup, prior to the structuration of the 150-nm thick Al by photolithography and lift-off techniques, the nitrate-based precursor was deposited on the oxidized wafer and thermally treated.

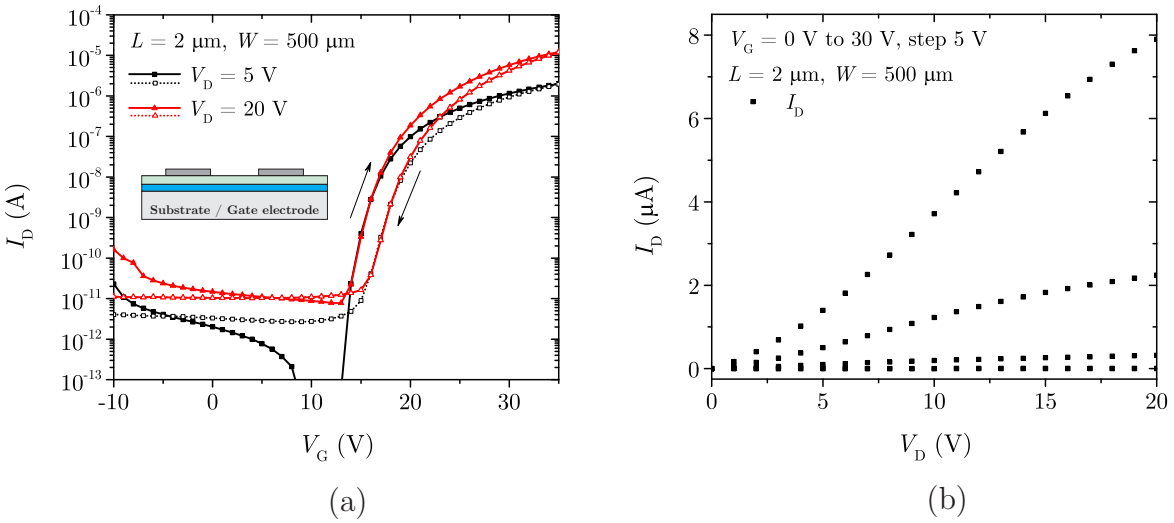


Figure 4.2: Input (a) and output (b) characteristics of a ZnO TFT with the deposition of one layer of the nitrate-based precursor integrated in an inverted staggered setup using lift-off technique. The inset depicts the cross-section of the TFT. Forward sweep: solid / backward: open.

The $I-V$ graphs for the inverted staggered setup are presented in Figure 4.2. The V_{ON} is equal to 14 V ($V_T = 20$ V), field-effect mobility, I_{ON}/I_{OFF} ratio and S are about $0.02\,cm^2V^{-1}s^{-1}$, 10^7 and 1.2 V/dec, respectively. Comparing the transistors $I-V$ curves of both setups, inverted coplanar (Figure 4.1) and inverted staggered (Figure 4.2), it is possible to observe a significant increase of the drain current level when the staggered setup is employed. The shift of the transistor threshold was ascribed to the stress suffered by the semiconducting material during the drain and source structuration as well as to the possible diffusion of Al to the ZnO film in the coplanar counterpart, which changes the metal-semiconductor contact behavior. Different from the results achieved in [MAH+08, TBS+11, BSTS12], there is no clear saturation of the drain current in the output characteristics. Even employing an inverted staggered setup, a relative high contact resistance can be noticed by the analysis of the linear region of the output characteristics in Figure 4.2b. At high gate voltages, the semiconductor channel is fully formed and presents high conductance; thus, the contact resistance dominates and limits the drain current during the drain voltage scan. At low gate voltage, however, the channel resistance increases, hence the drain current depicts a better saturation effect. Indeed, by the employment of an inverted staggered structure, the contact quality between the drain/source electrodes and the semiconducting layer is improved. Nevertheless, as a lift-off technique was used, residues of photoresist, which were eventually not removed during the developing step, act as a barrier for the current flow increasing the contact resistance of the

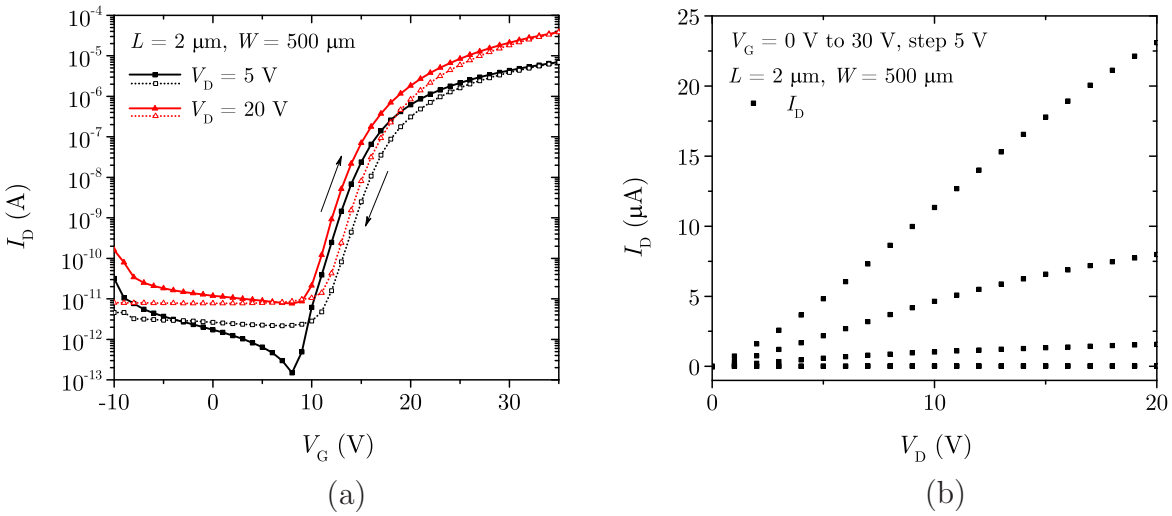


Figure 4.3: Input (a) and output (b) characteristics of a ZnO TFT with the deposition of 5 layers of nitrate-based precursor integrated in an inverted staggered setup. Forward sweep: solid / backward: open.

transistors [XOW+15]. Employing shadow masks as in [MAH+08, TBS+11, BSTS12], the ZnO layer will not be affected by further processing steps or by organic residues, yet the use of this technique may impose limitations for future scaling and mass-production. Moreover, in the integrated TFTs, the semiconducting layer formed by the nitrate-based precursor presents a good adhesion to the oxide layer for subsequent fabrication steps (lift-off technique) even at low annealing temperatures (150 ℃). This was not observed in the case of nanoparticulated ZnO layers when SiO_2 was applied as gate dielectric, unless a higher temperature step was performed to promote its adhesion [33].

Aiming at the improvement of the semiconducting layer, the precursor deposition and the curing step were repeated 5 times in order to fill possible cracks and gaps in the film, increasing its reliability [KYK14]. The electrical characteristics are shown in Figure 4.3. Through the deposition of multiple layers of the ZnO precursor, the impact of grain boundaries and of the ambient atmosphere is also expected to be reduced. Notably, the effect of the oxygen at the semiconductor surface is well-known to deplete the ZnO surface [Hir85]. One may expect that by employing a thicker ZnO layer (by multiple depositions and curing steps of the precursor), the depletion region (created at the semiconductor surface exposed to air) will not be extended to the dielectric/semiconductor interface. Since the TFT operation principle is based on the accumulation of carriers at this interface [SN07], the voltage when the transistor starts to conduct will be shifted to the left (negative values). This effect can also be observed by comparing Figure 4.2a and Figure 4.3a, in which

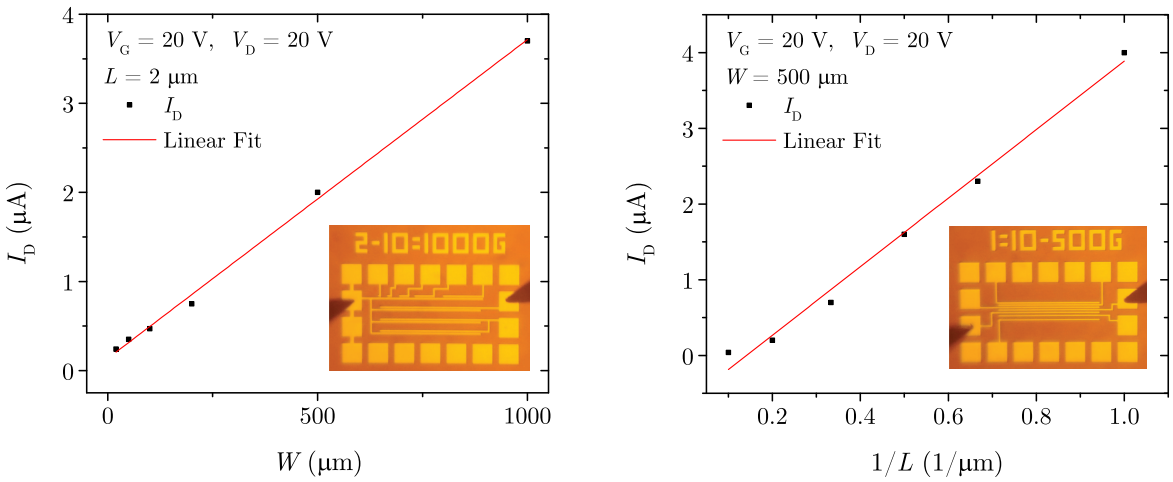


Figure 4.4: ZnO TFT scaling behavior depicting the linear relation of the drain current as a function of the transistor's (a) width and (b) length. The data are from ZnO TFTs integrated in an inverted staggered setup with 5 repeated deposition and curing steps of the nitrate-based precursor. The insets are optical microscope images of the structures during the electrical characterization.

V_{ON} and V_T are shifted from 14 V and 20 V down to 10 V and 16 V, respectively. Similar results were reported by Theissmann *et al.*, when a thicker ZnO layer was used [TBS+11]. Moreover, it is possible to observe that the drain current is slightly higher, which is related to the increase of the number of charge carriers not affected by trapped oxygen at the semiconductor surface [Hir85, VMJ07a], and to the improvement of the film morphology [TBS+11]. No significant changes in the off-current were observed when the thickness of the semiconductor was incremented by multiple precursor depositions [CLK+08, FBM12]. These observations reinforce the assumption that the semiconductor surface exposed to air is depleted and influences the dielectric/semiconductor interface. Nonetheless, it should be noted that as the multiple deposition steps were performed under ambient conditions, oxygen molecules can be trapped at the inter-layers of the ZnO film, which may induce variations in the TFTs characteristics.

The scaling properties of the integrated transistors were also investigated. In Figure 4.4 the drain current magnitude as a function of the transistor's width and length are plotted. A linear behavior, similar to that expected for standard MOSFETs, can be observed. The insets of Figure 4.4 depict optical microscope images of the structures during characterization.

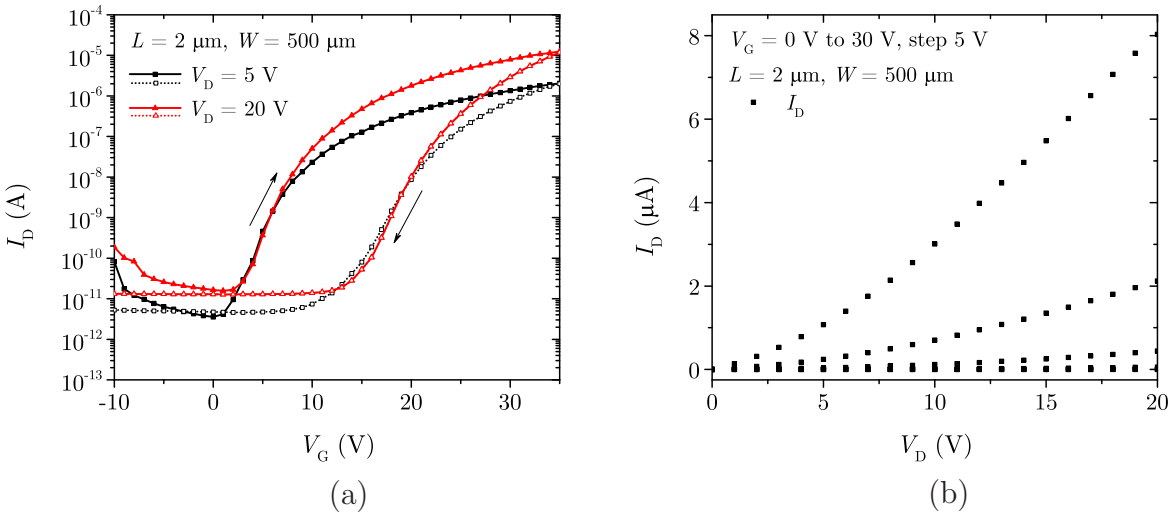


Figure 4.5: Input (a) and output (b) characteristics of a ZnO TFT with the deposition of one layer of the nitrate-based precursor in an inverted staggered setup after 7 min of UV-light irradiation. Forward sweep: solid / backward: open.

Based on the premise that the oxygen trapped in the ZnO layer can be removed by UV irradiation [Hir85, VMJ07a], the transistor with the characteristics presented in Figure 4.2 was exposed to UV-light ($\lambda = 365\,\text{nm}$ and $200\,\text{Wcm}^{-2}$) for 7 min in steps of 30 s of exposure time and 30 s of break. This was performed to prevent excessive substrate heating and possible damage, *e.g.* cracks, of the semiconducting layer. After the irradiation, the transfer characteristics of the transistor (Figure 4.5a) depicted a pronounced hysteresis ($\Delta V_{ON} = 11\,\text{V}$ and $\Delta V_T = 14\,\text{V}$) even though the output characteristics (Figure 4.5b), I_{ON}/I_{OFF} ratio, subthreshold swing and field-effect mobility suffered just minor variations. The forward threshold voltage was strongly shifted to the left (from $V_{ON} = 14\,\text{V}$ to 0 V and from $V_T = 20\,\text{V}$ to 10 V), which is in agreement with the desorption of the oxygen trapped at the ZnO surface. Nonetheless, damage on the SiO_2 may occur upon UV exposure [Lin94, TFK94] originating instabilities in the transistor operation. Furthermore, since no passivation was applied and the layer was still exposed to ambient atmosphere, oxygen adsorption was expected during the characterization, leading to performance degradation. Similar results were achieved by Xu *et al.* [XFH+12] before the application of polydimethylsiloxane (PDMS) as passivation layer on a ZnO TFT with comparable integration routine. Hence, prior to the application of such layer, a UV irradiation treatment can be performed to remove trapped oxygen at the semiconductor surface, reducing the transistor's operation voltage.

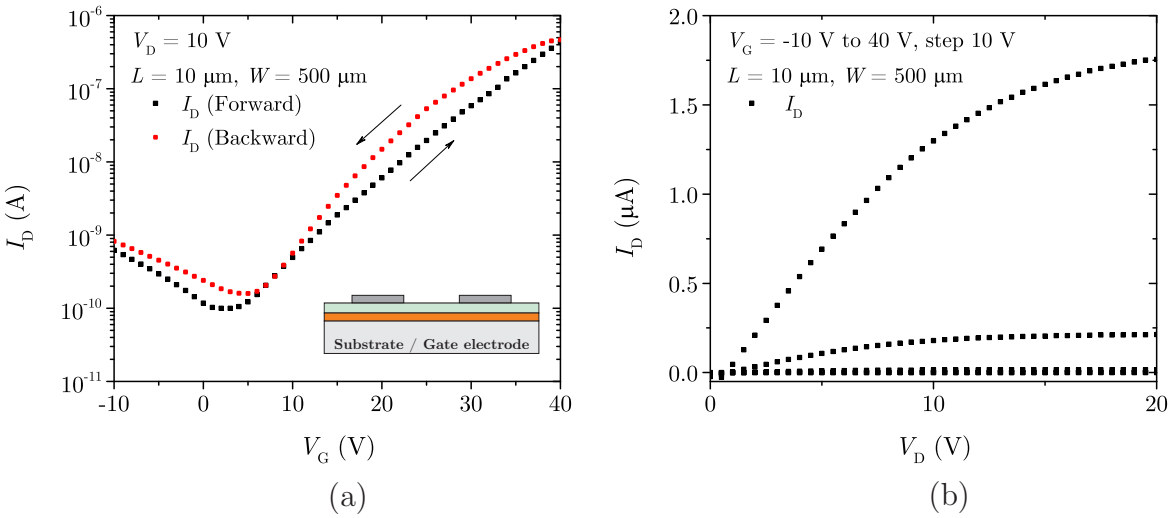


Figure 4.6: Input (a) and output (b) characteristics of a ZnO TFT with the deposition of 5 layers of the nitrate-based precursor in an inverted staggered setup employing the high-k resin as gate dielectric. Inset depicts the cross-section of the TFT.

Due to the encouraging results obtained employing a Si wafer as back gate contact and SiO_2 as gate dielectric, the nitrate-based precursor was evaluated also on the high-k resin. Therefore, a similar inverted staggered template was used, exchanging the SiO_2 for the nanocomposite. In order to achieve a better homogeneity, the deposition and curing processes of the nitrate-base precursor were also performed 5 times. The input and output characteristics are depicted in Figure 4.6. The extracted V_{ON} is approximately 5 V (V_T = 22 V), field effect mobility around $4 \cdot 10^{-4}\,cm^2V^{-1}s^{-1}$, I_{ON}/I_{OFF} ratio in the range of 10^4 and subthreshold swing of about 6.6 V/dec. Despite the reduction of the current levels, the transistors depict sufficient electrical performance and they are integrated at temperatures which are appropriated to some flexible substrates. Notwithstanding, the nitrate-based precursor contains oxidant agents in its composition that along with ammonia, also present in the precursor solution, are responsible for damaging the gate dielectric. As a result, agglomerations of a mixture of ZnO and high-k resin as well as a high defect density were observed on the semiconducting film. Further efforts were taken to apply the compound using spray-coating technique; however, its high volatility prevents a reliable process. Another observed effect was the time sensitivity of the solution, hence its degradation over time. Due to these limitations, to obtain a constant and reliable process as well as a stable ZnO film is complicated; therefore, the integration of TFTs applying precursors was discontinued.

4.2 Nanoparticulated ZnO TFTs

The advantages of employing a dispersion containing nanostructures of the materials to be applied for the integration of TFTs are innumerous aiming at a low-cost production on large area substrates. Besides their availability in different forms and sizes, the nanostructures can be dispersed in several solvent types, increasing their compatibility to specific processes and applications. In this section, the main results and analysis concerning ZnO nanoparticulated TFTs, either on rigid or on flexible substrates, are presented. The discussion starts with the charge carrier transport mechanism in nanoparticle networks, which is strongly affected by grain boundaries and by conduction through percolation paths. Secondly, nanoparticle-based transistors on rigid substrates are presented. They were studied in order to optimize the integration process and to provide comparative results for the subsequent integration on flexible substrates. Aiming at an improved performance, the transistor setup was modified, which leads the reader to the next chapter, where inverter circuits and ring oscillators are addressed.

4.2.1 Transport Mechanism

The integration of transistors using nanoparticle dispersions has, indeed, advantages concerning low-cost production and the application of methods for large area substrates. However, the employment of a nanoparticulated semiconducting film creates a network which forms preferable current paths; hence, the transport mechanism is commonly governed by the percolation theory [Meu99]. Although the formation of this network as well as its effects are enhanced when nanoparticles are used, one should notice that polycrystalline semiconducting films integrated using sputtering techniques or a precursor solution also give origin to a conduction through grain boundaries and preferable paths for the current flow [HYC$^+$08, GPF$^+$06]. Therefore, the effects observed for a nanoparticulated film can also be observed in those films, though their occurrence and their influence on the transistor's characteristics may differ.

Albeit the transport through percolation paths is generally observed in non-crystalline materials, crystalline semiconductors also present this kind of conduction based on an uneven energy potential distribution in the material. In modern nanoscaled MOSFETs, there is an irregular transport of electrons through the transistor channel mainly due to random dopant fluctuation, which also forms percolation paths for the current flow

[dWB06, BWd09]. The capture and emission of charge carriers by defects (traps) in a path affect the current flow electrostatically, modifying the transistor current level. This trap activity creates a step-wise behavior in the drain current called Random Telegraph Signal (RTS). The occurrence of a RTS is based on stochastic processes and its measurement depends on the traps capture and emission time constants, and on controlled and non-controlled system variables, hence a reliable prediction of its incidence is complicated. In this study, despite the relative large transistor size, similar current fluctuation takes place in a nanoparticulated ZnO TFT due to the semiconductor network characteristics.

Despite all the efforts for achieving high performance TFTs using nanoparticulated semiconductors, it is still jeopardized by the nanoparticle interconnections quality, which limits the carrier transport through the film. These connections could be improved by a high-temperature treatment of at least 400 ℃ [LJK+07]; however, this is inappropriate for the flexible electronic technology. The use of smaller nanoparticles (around a few nanometers) leads to a more uniform layer with an even charge carrier distribution at the gate dielectric/semiconductor interface [OMNH08, OH10]. Nonetheless, a rise in the number of interparticle connections occurs, increasing the film resistance, resulting in a lower on-state current. Additionally, the nanoparticulated film strongly interacts with the ambient atmosphere due to the large surface area of nanocompounds [XPST00, FL05]. Simultaneously, since the electron's flow is based on percolation paths in semiconductor films integrated using nanoparticles [Meu99], traps located at critical paths influence the device current, creating a discrete fluctuation in the transistor current when it is characterized over time [dWB06].

Figure 4.7 displays a section of the measured drain current as a function of time for fixed gate and drain voltages. In this stress test, it is possible to observe (I) a continuous increase of the drain current, which is ascribed to the reorietantion of dipoles in the gate dielectric and to desorption of molecular oxygen at the ZnO nanoparticles, and (II) the presence of fluctuations in the drain current[16]. This current fluctuation is similar to the one observed in modern MOSFETs, for which the emission and capture of charge carriers by traps are the main cause for such step-wise current behavior [dWB06, WCV+14]. Random dopant fluctuation creates percolation paths for the current flow, and traps located at particular current paths give origin to discrete current fluctuations [SIET07, ABBD03]. This noise causes problems, mainly failure of SRAMs and of flash memory and malfunction

[16] The results regarding the study of the RTS in ZnO nanoparticle TFTs were partly published in [28] and [29].

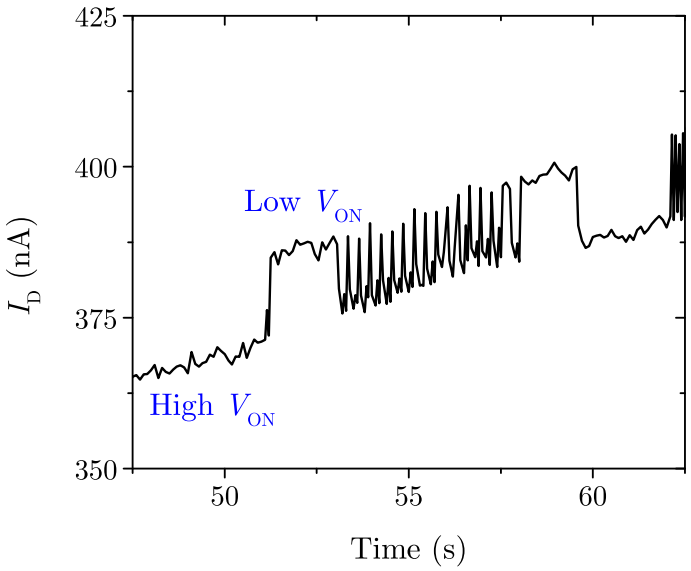


Figure 4.7: ZnO nanoparticle-based TFT under stress test affected by a single active trap depicting current fluctuations. The two current level states can be modeled as a variation in the turn-on voltage.

of micro-meso nanodevices [dLW11]. Because of their small dimensions, memory cells are commonly one of the first devices to be affected by this reliability issue. In the context of ZnO TFTs, the fluctuation of the drain current over time would affect the brightness of each pixel in an emissive active-matrix organic light-emitting diode (AMOLED), for instance [Con10]. To avoid nonuniformities in the display, the drain current should be roughly constant over time and, thus, trapping effects should be minimized.

For MOSFETs, this drain current fluctuation can be modeled as a momentary variation of the applied gate voltage. For device modeling, the RTS may also be expressed as a variation of the transistor's threshold voltage and it can be added as a parameter for circuit analysis [BWd09]. When the trap is electrically neutral, *i.e.* empty, the transistor is modeled as a low-threshold voltage state, in which the drain current is higher; likewise, when the trap is electrically charged, *i.e.* occupied, the transistor is in a high-threshold voltage state, in which the drain current is lower. For the ZnO nanoparticle TFTs, these two current levels can be represented as low-turn-on voltage state and high-turn-on voltage state, for instance, which is analogous to the modeling technique used for MOSFETs.

Concerning the traps themselves, they are commonly characterized by their mean capture and emission times as well as by their influence on the transistor behavior. The amplitude of the current fluctuation is characteristic of each specific trap, it is not sta-

tistically distributed as the capture and emission times [MS98]. Due to the non-uniform current flow in the transistor (percolation paths), each trap will have a different effect on the drain current depending on the current density at each part of the channel region. A trap located at a path with a higher current density will have a higher influence on the transistor current than one located at a low current path [MS98]. Conjointly, the trap position along the transistor source-drain line as well as the distance from the channel layer (distance from the semiconductor/gate dielectric interface) affects its influence in the current fluctuation amplitude [BWd09]. RTS is often detected in nanoscale MOSFETs, because a single trap will have a larger influence on the transistor current. The fluctuation steps in the drain current are predicted to increase as both the transistor's length and width decrease [KGR+10]; nevertheless, for state of the art MOSFETs, they are commonly in the scale of a few percent of the drain current [Rei14]. In the ZnO TFT integrated in this study, the observed amplitude of the current fluctuation ranged from 5% to 10% of the drain current despite the relative large transistor dimensions (channel length on the order of microns). The low temperatures employed on the nanoparticles produce a relatively porous semiconducting film that contributes to the formation of percolation paths. As a result of this conduction mode, active traps located in the nanoparticle network or at the gate dielectric/nanoparticle film interface may induce similar current fluctuations. Considering that the current in the ZnO nanoparticle transistor is in the order of μA, the blockage of a path may cause a fluctuation in the same order of magnitude.

Similar to MOSFETs, the trap location in the TFT channel plays an important role in the amplitude of the drain current fluctuation. Therefore, one can expect that the trap location in the nanoparticle network will also interfere on the fluctuation amplitude of the transistors integrated in this study. Figure 4.8 depicts a schematic nanoparticle network. In an average device, a denser network with a higher number of conducting paths is expected. Considering that traps located in high current density paths have higher influence in the transistor current [MS98], an active trap located at A will have less influence on the transistor current than the trap located at B, assuming that the path where B is located presents a lower resistance. Conjointly, interconnections of nanoparticles are susceptible to be more sensitive to the capture and emission of traps. In the study of Morrison [Mor81], the interconnections were reported as the main cause for the conductance variation in pressed/sintered ZnO films when the samples were exposed to molecular oxygen. For this reason, the trap located at B will also produce higher current fluctuations than the trap located at C, because the trap B is located at a nanoparticle

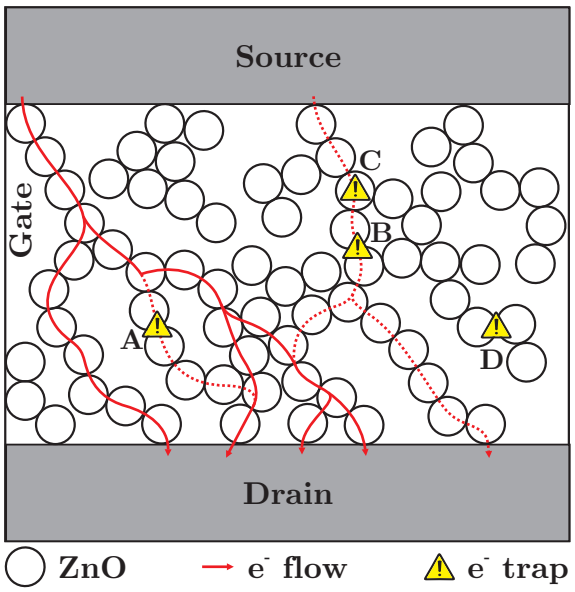


Figure 4.8: Electron flow under traps activity in a schematic nanoparticle network.

interconnection. Likewise, an active trap located at D will have almost no influence on the transistor current, since this trap is not located in an active current path.

Multiple active traps are also observed in a measured ZnO TFT; Figure 4.9 depicts the influence of at least three active traps during the stress test. The discrete fluctuation "a" from Figure 4.9 could be related to the trap located at A from Figure 4.8, for instance; the fluctuation "b" could be attributed to the trap located at B; and the fluctuation "c" to the trap located at C. This reinforces the assumption that the activity of different traps are responsible for distinct current level fluctuations. Additionally, the discrete current is a steady behavior, in which it is possible to clearly observe the capture and emission of particular traps. The trap activity does not damage the nanoparticle network or break a current path down, it just electrically reduces or even entirely blocks the current flow at a specific point in the nanoparticle network. Similar effects were already reported to occur in carbon nanotubes devices; in this case, discrete current fluctuations up to 60% of the total device current were observed and ascribed to trap activity [LBK+05]. This result emphasizes that the discrete current fluctuation has its origin from the capture and emission of traps and not from a measurement-induced noise. The occurrence of a RTS depends on the nanoparticle network and on the device configuration, as well as on the measurement conditions (*e.g.* temperature, humidity, applied voltage and sampling time); therefore, it is hard to predict the exact moment of its occurrence. For example, in the transistor characterized in Figure 4.7, the first discrete fluctuation observed occurred at around 50 s,

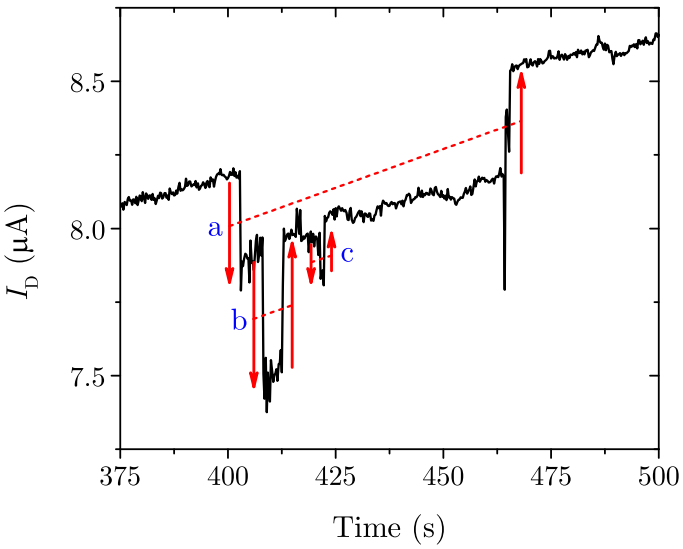


Figure 4.9: ZnO nanoparticle TFT affected by multiple active traps depicting different current fluctuation amplitudes.

whereas in the stress test depicted in Figure 4.9, trap activity started after 400 s. Factors like the instabilities in and at the gate dielectric and the interaction of the semiconducting material with the ambient atmosphere, as adsorption/desorption of molecular oxygen and humidity, strongly affect the transistor's electrical characteristics. Moreover, these effects can mask the traps activity during a transient period. Nonetheless, the observation of capture and emission of carriers are stochastic processes, hence identically integrated transistors will have a different trap activity behavior. Conjointly, traps located near the drain and source metal electrodes will also influence the metal/semiconductor interface in addition to the electrostatic effect on the semiconducting layer. Since these contacts are partially responsible for the TFT function [HYC+08, BL07, SN07], they are also a critical site concerning trap activity; therefore, the contact resistance may vary in time. Nevertheless, in TFTs, the contact quality is mainly affected by the transistor setup (staggered or coplanar), as already discussed in this study and shown in the literature [BL07, PCNF04, FBJ+09].

4.2.2 ZnO Nanoparticle TFT on Rigid Substrates

In order to optimize the integration process and to perform a more accurate analysis of the ZnO nanoparticle TFTs, devices were initially integrated on rigid substrates, either oxidized silicon or glass wafers. In this way, the additional variability associated to flexible

substrates was avoided. Nevertheless, integration techniques compatible to such substrates were employed, ensuring that the process is transferable to polymeric templates as described in Section 3.6. Based on the improved contact quality between the drain/source electrodes and the semiconducting film observed in inverted staggered setups, and aligned with prior research done in the Sensor Technology Department − Paderborn University − Germany [6], [Wol11], these setups, using PVP as gate dielectric, were firstly integrated and characterized.

Hysteretic behavior was already observed in organic and inorganic TFTs when employing PVP as gate dielectric [LKK$^+$07, FBJ$^+$09, VOLL04] (see Section 3.3.1). Lim *et al.* reported that the use of PVP as gate dielectric may influence the turn-on (threshold) voltage, shifting it according to the sweeping direction of the gate voltage in organic transistors [LKK$^+$07]. Faber et al. proposed that the emission and capture of positive charges by traps located in the ZnO nanoparticles/PVP interface cause the hysteretic behavior [FBJ$^+$09]. However, that model [FBJ$^+$09] does not explain the reason for the drain current increase when the gate voltage sweeps backward, neither the inversion of the hysteresis direction when the transistor is heated up. Such behavior was observed in the transistors fabricated in this study, as discussed later in this subsection.

Considering the PVP-based gate dielectric, the presence of hydroxyl (OH^-) groups changes the surface character from nonpolar to polar [JDWM05, LKK$^+$07]. Also, polymeric dielectrics, which contain a significant amount of hydroxyl groups inside or at the surface, are responsible for hysteresis in organic transistors as well as for a higher gate current leakage [LKK$^+$07, LKS$^+$06, KJJ$^+$08]. The explanation proposed for the hysteretic behavior of TFTs employing PVP as gate dielectric is based on [VOLL04, HLK$^+$06, HOH$^+$08], in which a hysteresis mechanism for pentacene-based TFTs is discussed. The slow polarization of dipoles, such as hydroxyl groups in the PVP bulk, reoriented by an applied electric field, was considered as the main reason for the observed behavior.

Figure 4.10 shows the trapping mechanism in the polymeric gate dielectric. Moreover, it is possible to observe the dipoles in the PVP bulk and the electron traps associated with the OH^- groups at the semiconductor/dielectric interface. Most of the defects in this polymeric dielectric are related to a non-complete polymerization due to a partial cross-linking reaction. Therefore, the direction of the hysteresis, considering the PVP influence, will be determined by the dominant mechanism in the device depending on measurement

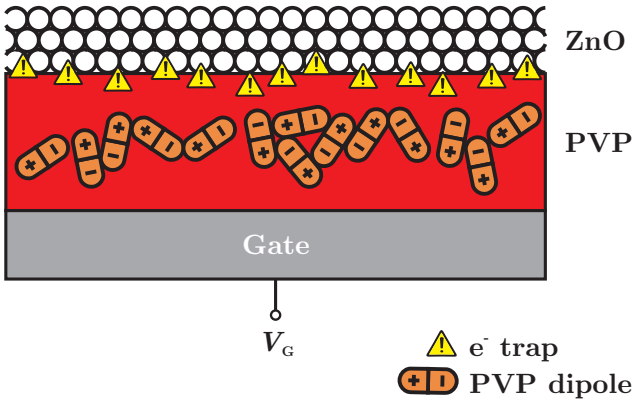


Figure 4.10: Trap mechanism in a ZnO nanoparticle TFT with PVP as gate dielectric. Adapted from [VOLL04, HLK+06, HOH+08].

and processing conditions, such as annealing temperature and duration, concentration of cross-linker agent, and dielectric thickness [VOLL04, LKS+06, HLK+06, HOH+08].

Traps at the nanoparticles may also play a vital role in the hysteresis. In early studies, Hirschwald reported the upward band bending by ionosorbed negatively charged oxygen molecules at the surface and at grain boundaries of the ZnO films [Hir85]. Adsorbed oxygen molecules located at the surface capture free electrons from the ZnO, reducing its conductivity [Hir85, JWS+08, VMJ06, WSGG10]. The desorption of the oxygen molecules upon UV illumination is associated with a generation of electron-hole pairs. The generated holes migrate to the surface and release the adsorbed oxygen molecules, increasing the concentration of free electrons in the ZnO film. As explained by [VMJ07a, VMJ07b], in addition to the UV interaction, it is also possible to induce the desorption of oxygen through the application of bias (voltage) or by the injection of positive charges through the metal/ZnO film contact [VMJ07a]. The oxygen trapping mechanism in nanoparticulated ZnO is depicted in Figure 4.11, representing the increase of free charge carriers (electrons). The interaction of the nanoparticle with the atmosphere is highlighted by the large surface area of nanomaterial compounds [XPST00] and its effects may influence the entire bulk of the ZnO film [JWS+08].

The device with PVP as gate dielectric[17] presents a highly pronounced anticlockwise hysteresis in the transistor transfer curve at room temperature when the gate voltage is scanned from $-10\,\mathrm{V}$ to $20\,\mathrm{V}$ and vice versa, as shown in Figure 4.12a. The hysteresis can be reproduced in the same transistor, as well as in other transistors integrated using

[17] The results regarding the study of the ZnO-based TFTs employing PVP as gate dielectric were partly published in [9] and [38].

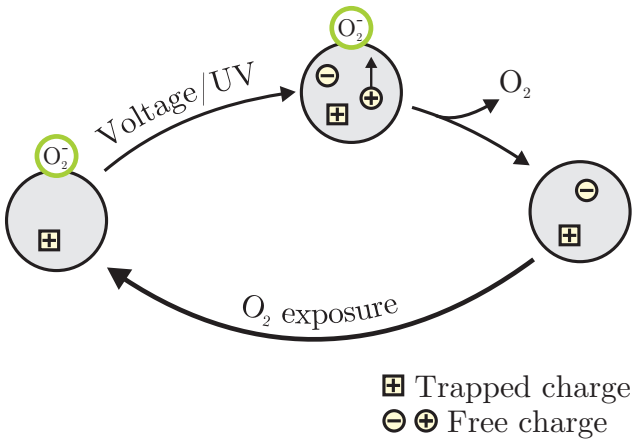


Figure 4.11: Oxygen trap mechanism in nanoparticulated ZnO. Adapted from [VMJ07a].

this process, under similar environmental conditions. In Figure 4.12b, it is possible to observe 15 transfer curves of different transistors (plotted in the same graph) showing that the hysteretic characteristic is highly reproducible among devices. The transistors' performance is strongly dominated by the hysteretic behavior. The V_{ON} is shifted from 0.6 V to −3.6 V during the forward and backward sweep of the gate voltage, whereas the V_{T} extracted by the linear extrapolation of the drain current is shifted from 9.2 V to −2.7 V. The μ_{FE} is around $6 \cdot 10^{-3}\,\mathrm{cm^2V^{-1}s^{-1}}$, the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio is of the order of $5 \cdot 10^5$ and S about 0.5 V/dec.

The polarization of the PVP is the key factor in the hysteresis depicted in Figure 4.12. The dipoles slowly become oriented by the applied gate voltage, enhancing its effect (the effective potential will be the result of the applied voltage and the amount of polarization); therefore, increasing the drain current even when the gate voltage starts to sweep backward. In order to turn off the transistor, a lower gate voltage is required. The orientation of dipoles in the polymeric material was predicted to be a slow process [HLK+06, HOH+08], which is in agreement with the observed current increase, despite the invariant bias voltage, as shown in Figure 4.13. A time constant of about 120 s was extracted considering a first-order exponential function. This result is consistent with the hysteresis direction presented in Figure 4.12. Moreover, the slow polarization reinforces the drain current rise when the gate voltage is swept back. An increment in the drain current at fixed electric bias was also reported by [FBJ+09]. Additionally, in [FBJ+09], the stress test was performed with different gate voltages, too. By applying higher gate voltages, the drain current increases at a higher rate [FBJ+09], which indicates that the

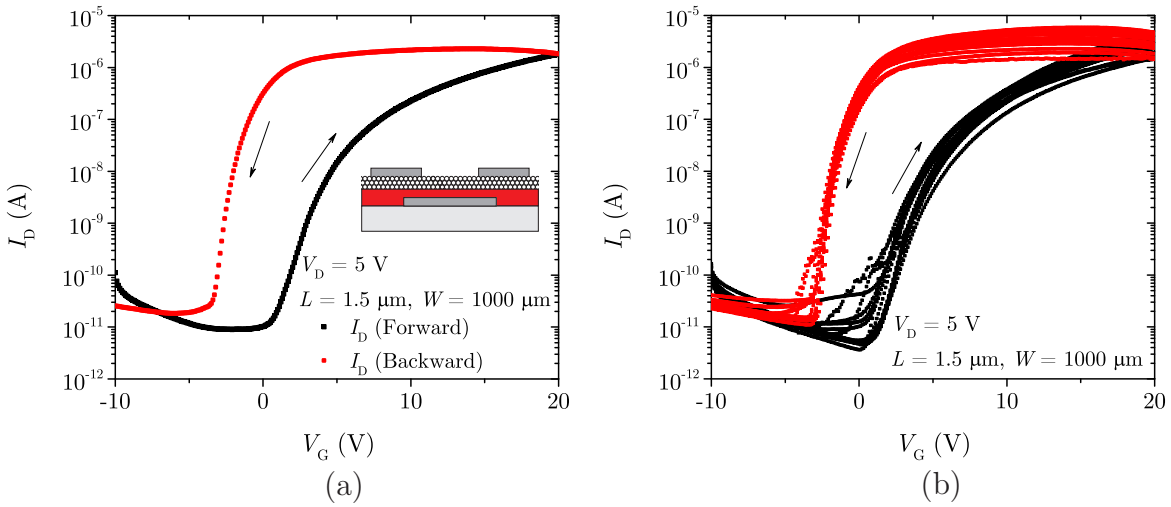


Figure 4.12: Transfer characteristics (a) of an inverted staggered ZnO nanoparticle TFT using PVP as gate dielectric at room temperature. The graph (b) shows the transfer characteristics of 15 different devices in order to depict the reproducibility of the hysteresis. The inset depicts the cross-section of the TFT.

polarization of PVP occurs faster due to the higher perpendicular electric field interacting with the PVP dipoles.

As discussed in the previous subsection, the electron transport mechanism in nanoparticulated ZnO films is based on percolation paths [Meu99]. Hence, the discrete current observed in Figure 4.13 is attributed to the capture and release of carriers by traps located in a specific current path in the nanoparticulated film. This process electrostatically affects the transistor and, consequently, its current [KGR+10, MS98, dWB06, SCS+09]. Assuming an electron trap located in one specific current path in the ZnO nanoparticle network, the transistor current decreases when the trap is occupied. When, however, the trap vacates, the current increases, resulting in discrete fluctuations of the drain current [MS98, SCS+09].

In the output characteristics of the TFT shown in Figure 4.14, it is not possible to see a clear saturation regime of the drain current. The low current levels observed as well as the non-saturation behavior are ascribed to the slow polarization effect of the gate dielectric. Therefore, during the increment of the gate voltage for each of the output curves extraction and during the scanning of the drain voltage itself, there is insufficient time for the orientation of the dipoles, which limits the transistor current and the occurrence of the saturation regime. Additionally, impurities, *i.e.* photoresist residuals, that can be situated between the drain/source electrodes and the nanoparticulated layer act as a

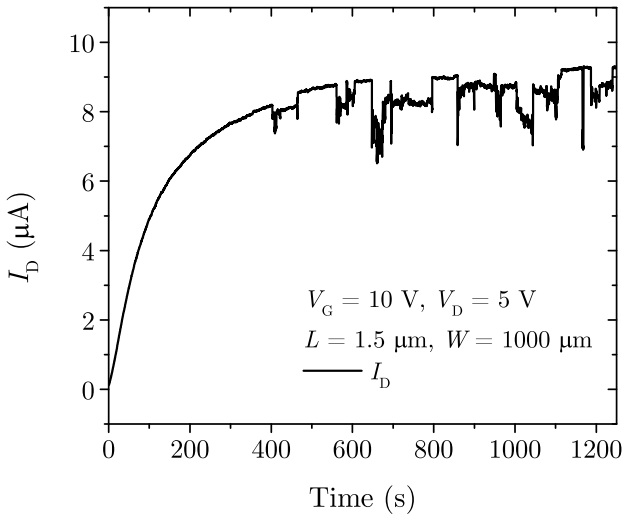


Figure 4.13: Stress test at room temperature in a ZnO nanoparticle TFT using PVP as gate dielectric.

charge carrier barrier. Although cleaning of the layer surface in organic solvents enhances the contact properties [JP06], this process cannot be employed, because it has to be performed in presence of the photoresist (after the development), which would harm the resist in turn.

When a transistor is characterized using multiple cycles measurements (with a 3-s delay between each cycle), it is possible to observe an increase of the drain current at the end of each successive forward sweep, as shown in Figure 4.15. This result is in agreement with the stress test, in which the drain current increases due to the polarization of the polymeric dielectric. Moreover, in the first electrical characterization, the "forward" curve is shifted to the left compared to the other two measurements, which can be attributed to an initial random orientation of the PVP dipoles. Finally, as also depicted in Figure 4.15, the "backward" curve is left shifted at subsequent characterization, indicating that a greater number of PVP dipoles are being oriented by the applied electric field, and also a presence of residual polarization effect in the gate dielectric.

In Figure 4.16, a slower sweep rate[18] ($0.003\,\mathrm{Vs}^{-1}$) was used for the electrical characterization of the transistor. In comparison to the $I - V$ curve shown in Figure 4.12, the on-state current level is higher with the slower sweep rate, which is in agreement with the slow polarization of the PVP and the stress test depicted in Figure 4.13. Moreover, when the gate voltage sweeps backwards, there is enough time for a reorganization of

[18]Parameter delay time of the HP-4156A − Precision Semiconductor Parameter Analyzer was set to 60 s.

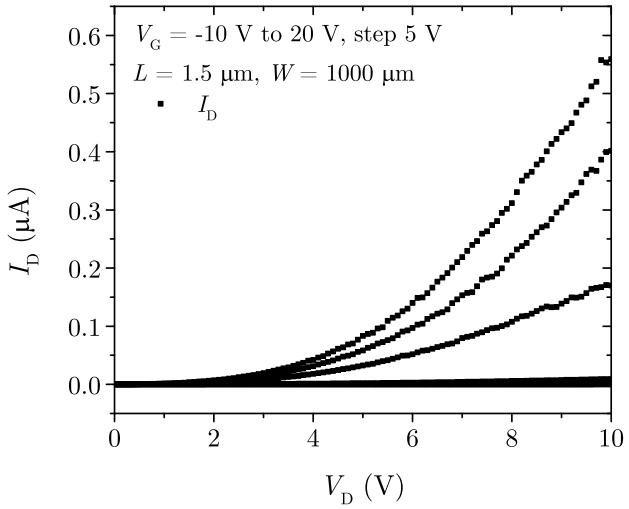


Figure 4.14: Output characteristics of an inverted staggered ZnO nanoparticle TFT using PVP as gate dielectric.

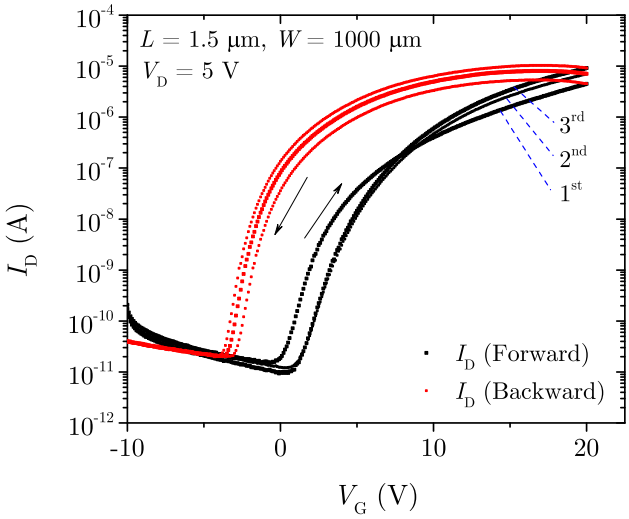


Figure 4.15: ZnO nanoparticle TFT transfer characteristics for multiples cycles with a 3-s pause between each measurement at room temperature.

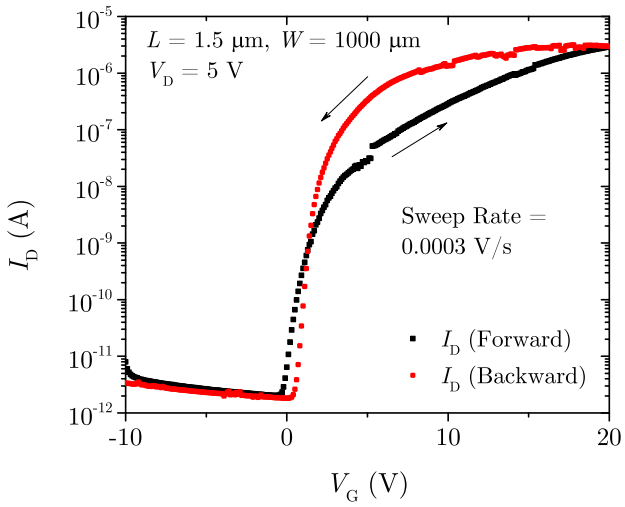


Figure 4.16: ZnO nanoparticle TFT transfer characteristic at room temperature with a sweep rate of $0.003\,\mathrm{Vs}^{-1}$.

the PVP dipoles, hence the hysteretic behavior is mitigated. Additionally, the electrical characterization of the transistor in Figure 4.16 presents similar step-like behavior as the one observed during the stress test, showing the trap activity effect during the extraction of the transfer and output characteristics.

Furthermore, in order to investigate the temperature dependence of the transistor hysteretic behavior, the TFT was heated to a specific temperature and then electrically characterized. This procedure drastically changed the electrical characteristic of the device, as shown in Figure 4.17. The direction of the hysteresis in the $I_D - V_G$ curve modifies from anticlockwise to clockwise. This behavior may be attributed to a change in the mechanism dominating the hysteretic characteristic. While at lower temperatures the PVP bulk polarization is the main reason for the hysteresis, when the temperature is increased, the dipoles in the polymer become randomly oriented and/or partially annealed [OM03] resulting in a reduction of their effects upon transistor characteristics. On the other hand, at higher temperatures the trap activity may increase. At this point, the dominant phenomenon is the trapping of carriers in the nanoparticles and at the gate dielectric interface mainly caused by the OH^- groups. Traps located at the surface reduce the applied gate voltage and act as scattering centers for the electron transport, degrading the drain current specially when the gate voltage is swept backward [ZGK+93, OM03]. Moreover, the change in the hysteretic behavior is in accordance with the stress test at higher temperatures, as shown in Figure 4.18. The drain current degradation observed in

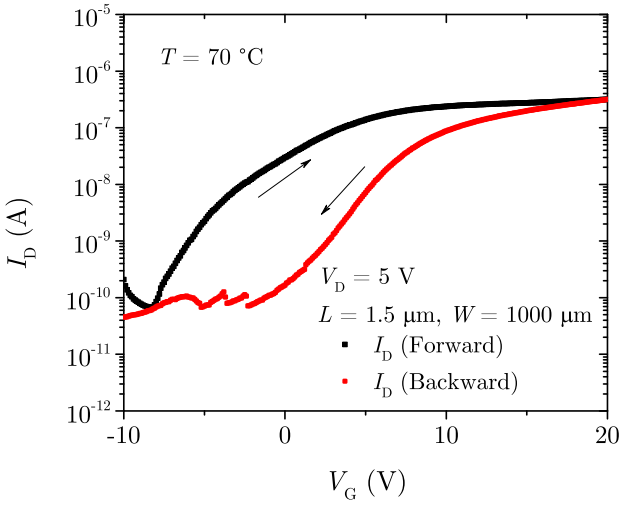


Figure 4.17: Transfer characteristics at 70 ℃ of a ZnO nanoparticle TFT using PVP as gate dielectric.

this case occurred at a higher rate (time constant of approximately 17 s) than the one at room temperature.

Considering the stress test at higher temperature shown in Figure 4.18, no discrete current fluctuation could be noticed. This may be related to the probability of a trap to be active at a determined scenario, to the influence of temperature on the capture and emission time constants of each trap or even to the capability of the measurement equipment to resolve faster traps.

Figure 4.19 shows the variation of the turn-on and threshold voltages as a function of temperature. It is possible to observe that the hysteresis changes its direction at around 45 ℃ − 55 ℃ and that the "forward" turn-on (threshold) voltage is more sensitive to temperature variations mainly due to the temperature dependence of the charge state of the interface traps. When the transistor is cooled down to room temperature, the hysteresis returns to its initial direction (anticlockwise).The I_{ON}/I_{OFF} ratio clearly decreases with increasing temperature, as shown in Figure 4.20. This may also be indirectly observed by comparing Figure 4.12 and Figure 4.17. The off-state current in Schottky diodes at the drain and source contacts is strongly correlated with the temperature, hence the leakage current through the barrier increases [RW88]. The on-state current level decreases because it is affected by electron trapping at the semiconductor/dielectric interface and by the weaker dipole orientation at higher temperatures.

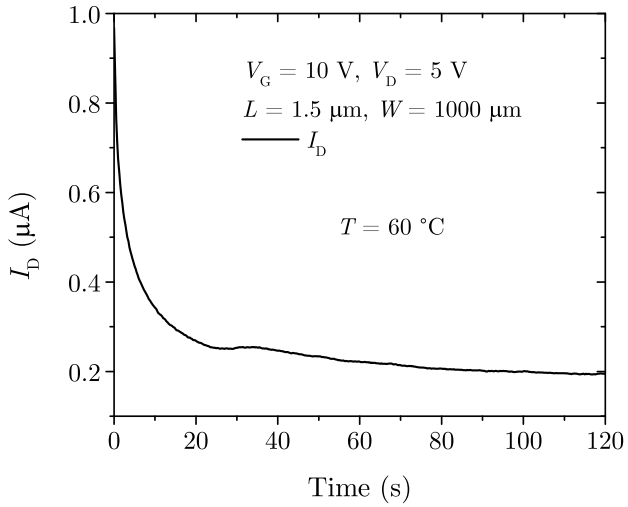


Figure 4.18: Stress test at 60 ℃ in a ZnO nanoparticle TFT using PVP as gate dielectric.

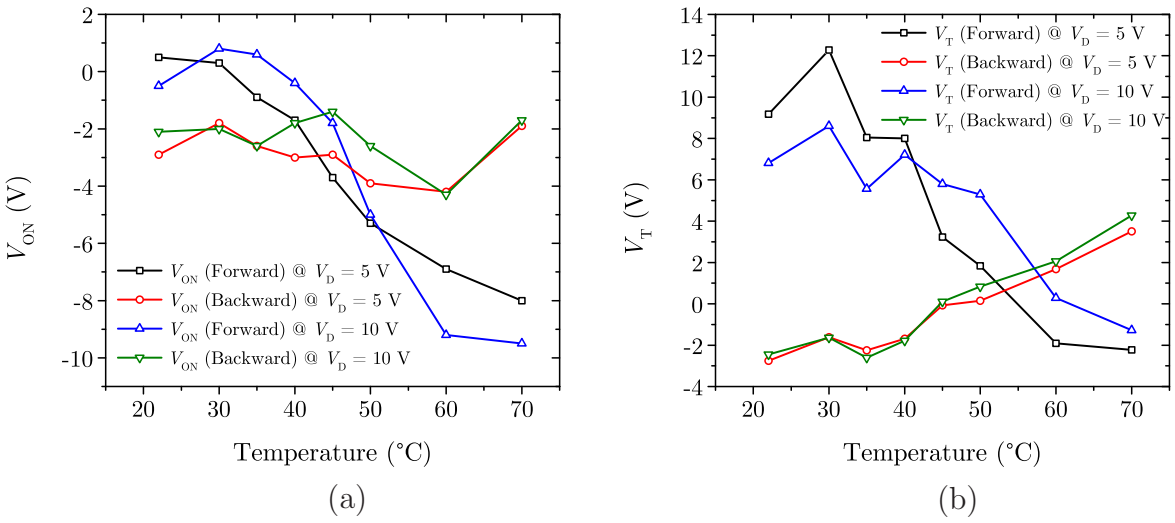


Figure 4.19: Turn-on (a) and threshold (b) voltage at different temperatures of ZnO nanoparticle TFTs.

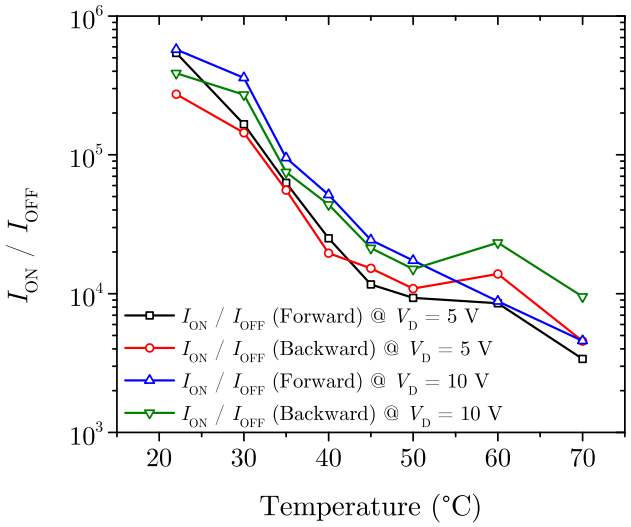
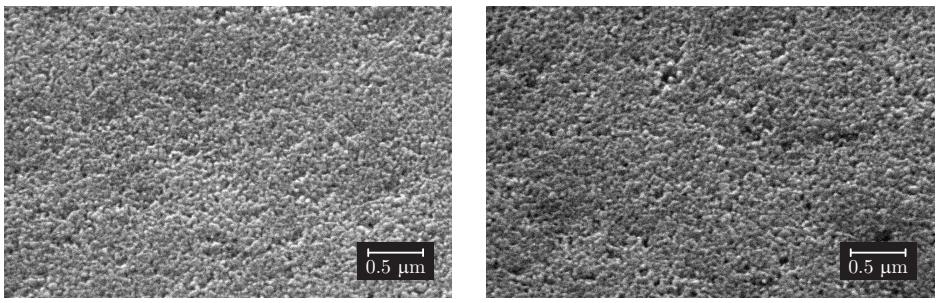


Figure 4.20: I_{ON}/I_{OFF} ratio at different temperatures of a ZnO nanoparticle TFT.

As described in [9] and [Wol11], the employment of PECVD-SiO_2 as dielectric layer in ZnO nanoparticle TFTs also gives rise to an anticlockwise hysteretic behavior in the transfer characteristics of the transistor. This effect reinforces the fact that the slow polarization of the PVP bulk is not the only mechanism responsible for the shift in the threshold voltage. The desorption of oxygen molecules increases the concentration of mobile charge carriers in the nanoparticles, hence increasing the transistor current; this process may explain the hysteresis direction observed in the transistor with silicon dioxide as gate dielectric. Conjointly, oxygen vacancies in the nanoparticles can act as mobile charged dopants. By applying an electric field, these dopants drift causing a hysteretic behavior, as observed in TiO_2-based memristor devices [SSSW08]. This effect was also discussed by [WSGG10] in a memristive device based on ZnO nanocrystals. Oxygen ions located near the Al/ZnO interface drift into the semiconductor bulk material or into the interface depending on the applied bias, increasing or reducing the number of oxygen vacancies and affecting the barrier for electron injection [WSGG10].

Another study [NCS+03] shows that a low-temperature PECVD-SiO_2 layer presents a higher defect density than thermally grown oxides. Such defects at the ZnO-film interface are mentioned as the reason for the presence of the hysteresis. Conversely, the anticlockwise hysteresis present in the transistor integrated in [Wol11] suggests that the oxygen trap mechanism dominates the traps at the SiO_2/ZnO interface which induces a clockwise hysteretic behavior [NCS+03]. During the stress test in the SiO_2-based device at room temperature depicted in [9], the drain current increases at first suggesting desorption of



(a) (b)

Figure 4.21: Scanning electron microscope images of ZnO nanoparticles layers (a) without and (b) with hydrothermal deposition of zinc acetate.

molecular oxygen trapped in the nanoparticulated ZnO surface, as well as supporting the hysteresis direction in the transfer characteristic. Subsequently, however, the drain current decreases, which is attributed to the electron trapping in the gate dielectric [CS08]. This result indicates that desorption of oxygen saturates over time, and that the trapping of carriers at the SiO_2 interface becomes dominant, reducing the drain current. In addition, this may explain the distinct results found by [NCS$^+$03, MAH$^+$08, BMHS10, TBS$^+$11].

A further analysis on the characterization of the hysteretic behavior on nanoparticulated ZnO TFTs using PVP and PECVD-SiO_2 as gate dielectric can be found in [38]. Additionally, the influence of the drain voltage in the hysteresis as well as a statistical evaluation of the TFT electric characteristics are also available in the aforementioned work.

Aiming at an improvement of the interconnectivity between neighboring nanoparticles and a reduction of the defect density, a hydrothermal decomposition of a zinc salt on top of the nanoparticles can be performed [LJK$^+$07, LJJ$^+$08, CKJ$^+$12]. Therefore, for the TFTs employing PVP as gate dielectric, the acetate-based precursor was spin-coated and cured after the deposition of the ZnO film[19]. Afterward, the drain and source electrodes were structured, as discussed in Section 3.6.1. Figure 4.21 presents scanning electron microscope (SEM) images of the nanoparticulated ZnO layer (a) without and (b) with the deposition of the precursor. No significant differences regarding the hydrothermal decomposition of the zinc salt could be seen and a regular surface was observed for both cases. Conjointly, it is possible to note the complexity and density of the ZnO nanoparticle network (percolation paths) that acts as active semiconducting layer.

[19]The results related to the acetate-based precursor on top of the ZnO nanoparticles were partially published in [34].

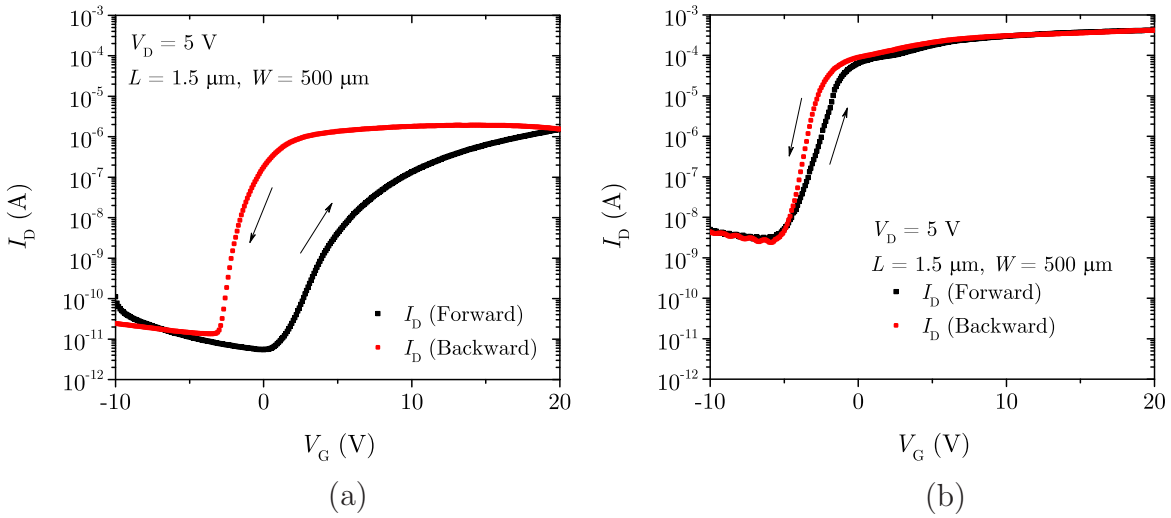


Figure 4.22: Transfer characteristics of ZnO nanoparticle TFT (a) without and (b) with the addition of the acetate-based ZnO precursor.

The $I - V$ curve of the ZnO nanoparticle TFTs with addition of the zinc precursor (Figure 4.22b) is presented next to the reference (without the acetate-based precursor) transistor (Figure 4.22a) in order to allow an easy comparison. It is possible to observe that a hydrothermal decomposition of a zinc salt leads to a device with better performance and to an almost complete vanishing of the hysteretic behavior in the transfer characteristics. Moreover, the turn-on (threshold) voltage is shifted towards lower values and a reduction in the hysteresis from $\Delta V_{\mathrm{ON}} = 4\,\mathrm{V}$ to $\Delta V_{\mathrm{ON}} = 0.1\,\mathrm{V}$ ($\Delta V_{\mathrm{T}} = 11.9\,\mathrm{V}$ to $\Delta V_{\mathrm{T}} = 0.9\,\mathrm{V}$) occurs. The results of the addition of the acetate-based precursor to the transistors indicate that the zinc salt is related to the improvement of the nanoparticles/PVP interface as well as of the interconnections between neighboring particles, reducing the trap density. Compared to the TFT without the ZnO precursor, an overall increase of the current level was observed, and also the expected increase of the field-effect mobility by two orders of magnitude. Mobility values of $0.7\,\mathrm{cm^2V^{-1}s^{-1}}$ were extracted from the transfer characteristics, whereas the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio and the subthreshold swing are unaffected with values of 10^5 and $0.5\,\mathrm{V/dec}$, respectively.

The performance enhancement and the significant reduction of the hysteresis were attributed to positive ions from the acetate-based precursor, which work as an electric shield over the traps. This mechanism was assumed to be the origin of the observed behavior since it was the "forward" turn-on (threshold) voltage that was substantially left shifted and also due to the drastic increase of the transistor off-state current. As described in Section 3.3.1, the low temperature employed (200 ℃) is insufficient for a complete synthe-

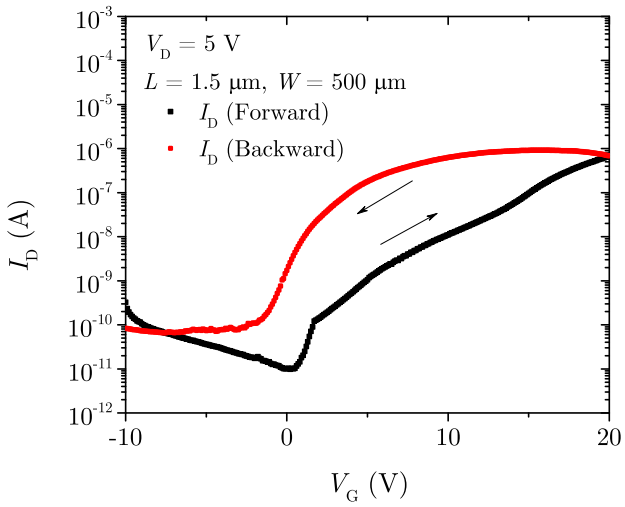


Figure 4.23: Transfer characteristic of ZnO nanoparticle TFT after aging and loss of the shielding effect.

sis reaction, leaving, therefore, free ions of the zinc salt in the semiconducting layer. Two weeks later, the transistors were characterized once again (Figure 4.23) and it was verified that the electric shielding achieved by the addition of the zinc precursor was no longer affecting the device. A hysteretic behavior similar to the one observed in non-treated transistors was noted. Additionally, the drain current level was lower and the transistor operation voltages (V_{ON} and V_T) as well as its characteristics were also similar.

Further investigations were performed applying the acetate-based precursor on the ZnO nanoparticle film; these tests were carried out employing oxidized Si wafers (Si wafer as gate electrode and SiO_2 as gate dielectric). Despite the variation on the deposition sequence and the evaluation of mixing both solutions (acetate-based precursor and nanoparticle dispersion) at different concentrations, a reproducible and effective procedure could not be achieved at low temperatures. Functional TFTs were observed when applying temperatures as high as 400 ℃, however, it restrains their application on polymeric substrates. Therefore, this approach was discontinued at least concerning the acetate-based precursor.

One of the main issues concerning the TFT instability, as already mentioned, is the hysteretic behavior, which has its origin in the slow polarization of dipoles found in the gate dielectric (PVP), in the high defect density in the semiconducting layer and in the interaction of the semiconductor material with the ambient air. In order to remove the instability originated by the incomplete cross-linking reaction of the polymeric (PVP)

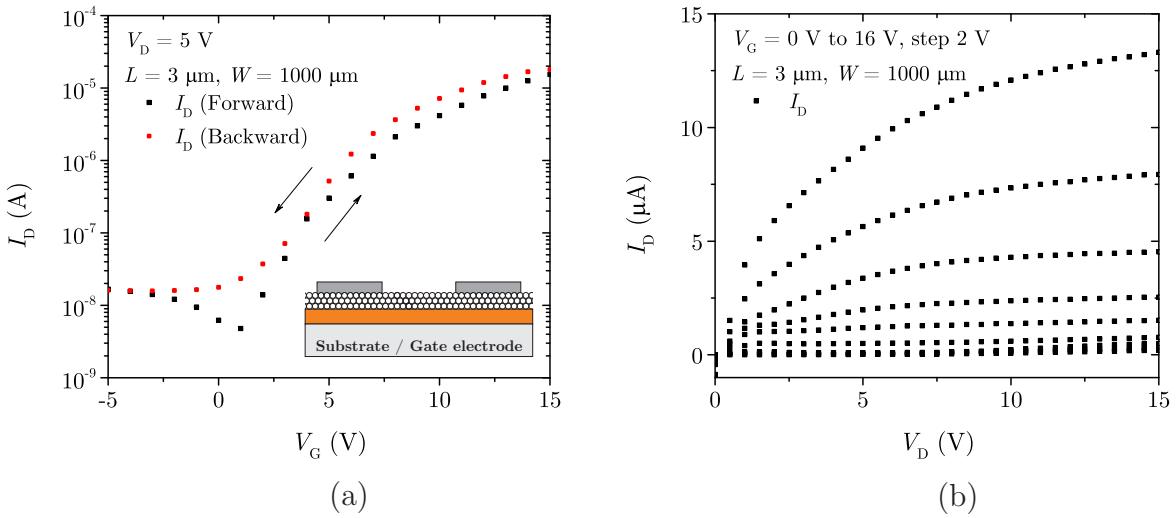


Figure 4.24: Transfer (a) and output (b) characteristics of an inverted staggered ZnO nanoparticle TFT with the high-k resin as gate dielectric and a Si-wafer as gate electrode. The inset depicts the cross-section of the TFT.

gate dielectric, the high-k resin described in Section 3.3.2 was investigated as a substitute. Along with the curing and cross-linking by a combination of low thermal treatment and UV irradiation, which enables its use on polymeric substrates, this gate dielectric has a high relative permittivity that increases the capacitive coupling between the gate electrode and the TFT active channel region.

First experiments were performed on a silicon wafer using an aluminum back layer to improve the contact quality to the gate electrode (Si) and to optimize the process prior to the integration of the template with structured gate. Figure 4.24 shows the input and output characteristics of a ZnO nanoparticle TFT employing the high-k resin as gate dielectric. The switching point of the transistor is adequate (around 0 V) and a small hysteretic behavior is observed. In such transistors, a relative high leakage current in the off-state of the transfer characteristics and in the output curves at low drain voltages was observed. This is related to the large overlapping area between the drain, source and connections electrodes, and the gate contact (entire Si wafer).

For the high-k resin, no significant variations on the operating voltages (ΔV_{ON}) were observed when the transistors were heated up, in contrast to the previously described TFTs with PVP as gate dielectric. The TFT transfer curves at room temperature (pre and post heating) and at 100 °C are shown in Figure 4.25 for comparison. Temperatures of about 200 °C cause irreversible damage to the device, whereas temperatures around 150 °C lead to a reversible increase of the transistor leakage currents. Since the flexible

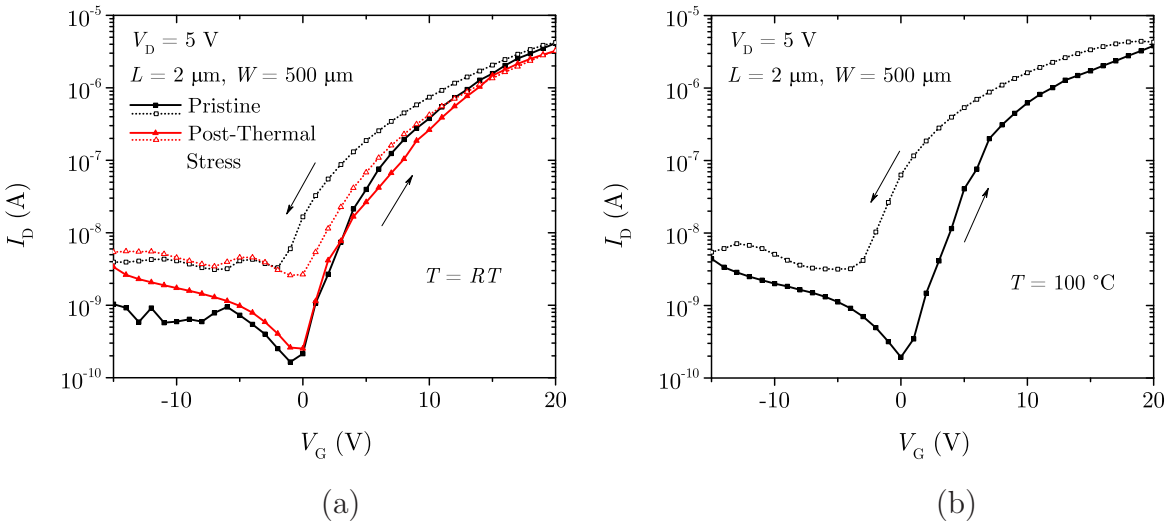


Figure 4.25: Temperature influence on the transfer characteristics of the ZnO nanoparticle TFT with the high-k resin as gate dielectric and a Si wafer as gate electrode (a) at room temperature and (b) at 100 °C. Forward sweep: solid / backward: open.

substrate later employed on the TFT fabrication does not endure high temperatures, the gate dielectric failure at around 200 °C is not a concern.

Based on the results achieved employing the high-k resin as gate dielectric, the TFTs were integrated applying structured-gate electrodes[20] following the procedure described in Section 3.6.1. Figure 4.26 shows an optical microscope image of the transistors during the characterization. In Figure 4.27 the transfer and output characteristics of the transistor directly after its fabrication are depicted. The transfer characteristic presents a minimal hysteresis (ΔV_{ON} and ΔV_T around 0.2 V) when the gate voltage is scanned from −7.5 V to 10 V and vice versa, even without a passivation layer and employing maximum fabrication temperatures of 150 °C. The V_{ON} is approximately −1.8 V, whereas the V_T extracted from linear extrapolation of the $I_D^{1/2}$ graph is approximately 2.2 V. The field-effect mobility is in the order of 0.1 $cm^2V^{-1}s^{-1}$, the subthreshold swing is around 1.2 V/dec, and the I_{ON}/I_{OFF} ratio is about 10^4. While the on-state current is believed to be limited by the interparticle transition resistances, the off-state current is constrained by the background carrier concentration [FBM12, Con10] and by the leakage current through the gate dielectric (around 10^{-8} A). Additionally, the Schottky contacts at the source and drain electrodes, which present higher leakage current than conventional p-n junctions, also influence the transistor off-state [WH10, SN07]. Conjointly, in Figure 4.27, it is possible

[20] The results regarding the study of the ZnO-based TFTs employing the high-k resin as gate dielectric were partly published in [8].

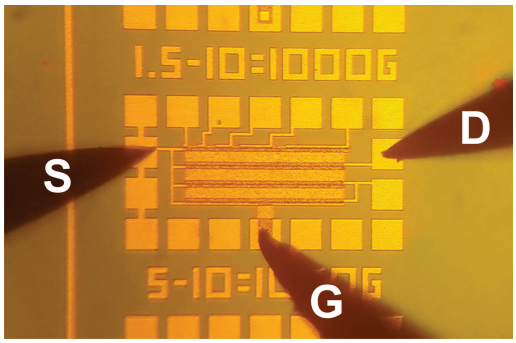


Figure 4.26: Optical microscope image of a set of transistors during the electrical characterization. S, D and G are source, drain and gate contacts, respectively.

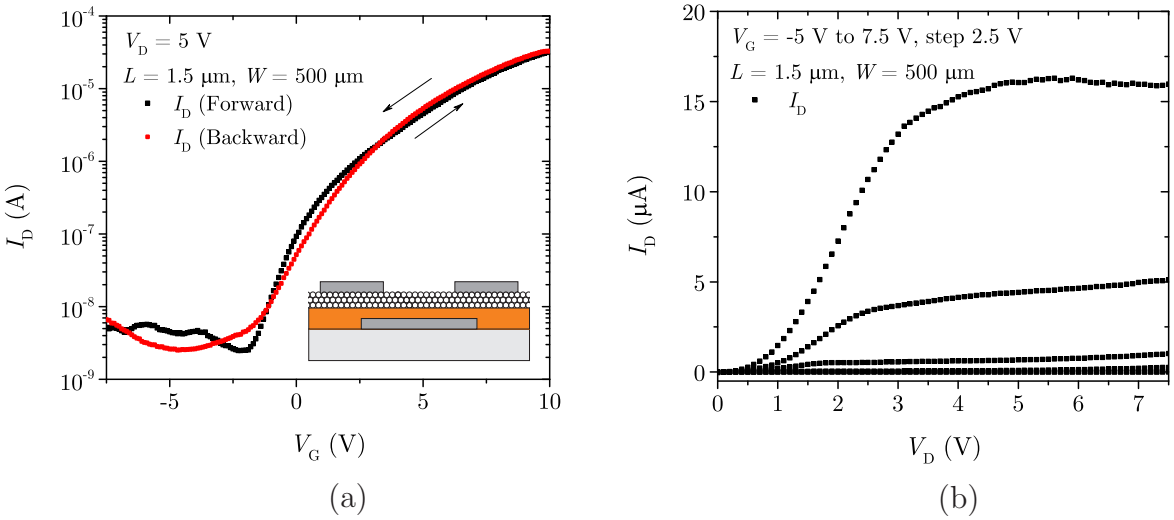


Figure 4.27: Transfer (a) and output (b) characteristics of a pristine inverted staggered ZnO nanoparticle TFT employing the high-k nanocomposite as gate dielectric. The inset depicts the cross-section of the TFT.

to observe the saturation of the drain current as well as the current modulation by the applied gate voltage in the saturation region.

In comparison to crystalline and polycrystalline materials, nanoparticulated films have a porous structure [FBM12, MAH+08, Meu99, LJJ+08]. The porosity of the film may pose challenges regarding scaling [VMM+04], especially when the nanoparticle size is in the same order of magnitude as the transistor length. The drain current as a function of the transistor width and length is plotted in Figure 4.28. It is possible to note that the transistor scaling behavior is similar to that of standard MOSFETs. The good scaling properties achieved in these transistors are ascribed to the nanoparticle dispersion, which is free of encapsulated nanostructures and of organic dispersant agents. These charac-

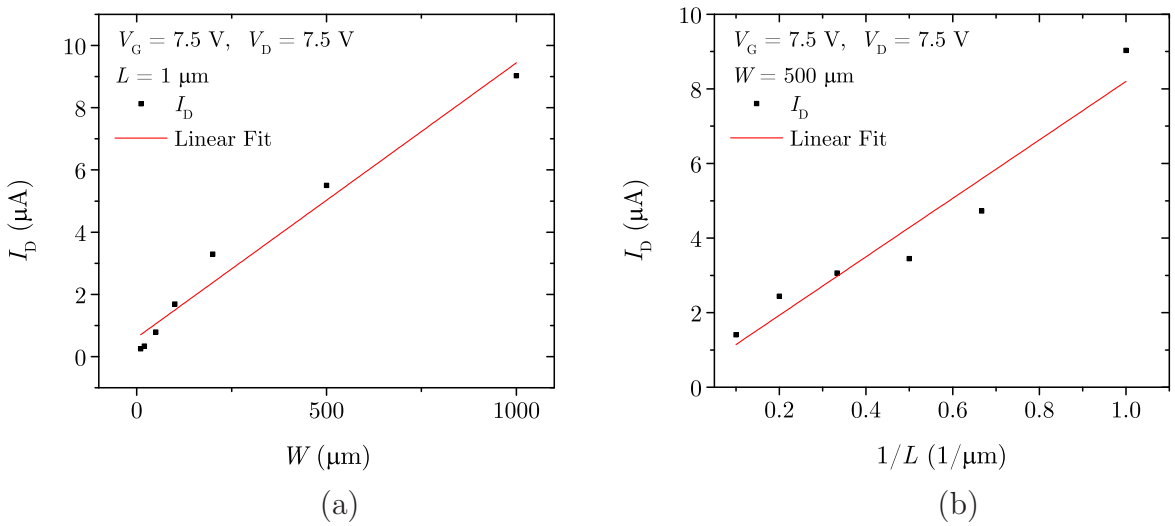


Figure 4.28: Inverted staggered ZnO nanoparticle TFT scaling behavior depicting the linear relation of the drain current as a function of the transistor (a) width and (b) length.

teristics enhance the nanoparticles contact quality, overcoming the film porosity, even in films treated at low temperatures.

Three days later, the transistors were characterized again to evaluate degradation effects. The transistor characterization, transfer and output curves are shown in Figure 4.29. This time, an anti-clockwise hysteresis ($\Delta V_{ON} = 5\,V$, $\Delta V_T = 3.2\,V$) in the transfer curves was observed. The "forward" and "backward" turn-on (threshold) voltages are $-4\,V$ ($2.6\,V$) and $-1\,V$ ($-0.6\,V$), respectively. Additionally, both the drain current level and the field effect mobility decreased about one order of magnitude. Such degradation was expected since no passivation layer was deposited. Previous studies [SKFN62, XPST00] have investigated the use of ZnO as gas sensor; therefore, one might expect that the nanoparticle layer would interact with the atmosphere, increasing or decreasing the carrier concentration in the semiconducting film [VMJ07a, Hir85, Mor81].

The onset of the current degradation and of the hysteresis was attributed to the adsorption of molecular oxygen at the nanoparticle surface, in which the oxygen reduced the carrier concentration in the semiconducting layer by trapping free electrons and depleting the nanoparticle surface, as described in the literature [Hir85, VMJ07a]. The direction of the hysteresis and the increase of the drain current, even when the gate voltage starts to sweep backwards, are considered to be related to a partial desorption of the oxygen from the semiconductor during the TFT characterization. In the literature, it is possible to find explanations for such desorption from the ZnO nanoparticle surface. UV irradiation, for

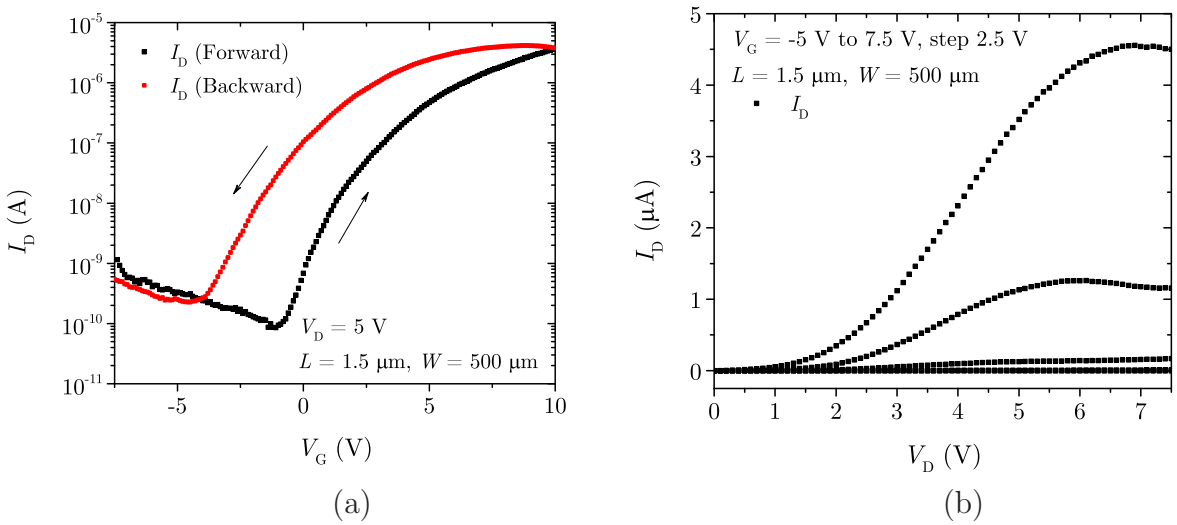


Figure 4.29: Transfer (a) and output (b) characteristics of a ZnO nanoparticle TFT after 3 days depicting degradation over time.

example, is reported to increase the carrier concentration in the semiconductor as its wavelength closely matches the ZnO band gap, generating electron-hole pairs [JWS+08, PJ12]. These holes recombine with the chemisorbed oxygen releasing it. Additionally, an applied electric field may affect the Al/ZnO contact characteristics through ion drift and subsequent adsorption or desorption of molecular O_2 at the semiconducting layer [WSGG10]. Verbakel *et al.* [VMJ07a] ascribed this desorption to positive charge carriers, either by injection via a metal contact or generated by UV-light irradiation. Conjointly, humidity at the nanoparticle surface may assist the release of oxygen. Morrison [Mor81] reported that physically adsorbed water leads to an unfavorable state for O_2 molecules trapped at the ZnO particles, which will desorb, increasing the carrier concentration in the semiconducting layer. In ZnO TFTs fabricated using vacuum techniques, the semiconductor film exhibits fewer grain boundaries as well as a smaller surface area when compared to nanoparticles. Additionally, it is generally thinner (around 50 nm), meaning that the semiconductor surface exposed to the ambient is closer to the dielectric interface. For this reason, the ambient atmosphere predominantly affects the gate dielectric/semiconductor interface, shifting the turn-on (threshold) voltage. Additionally, electron trapping at this interface is reported to have a greater impact in the transistor characteristics degrading the drain current, hence the hysteresis will show a clockwise direction [NCS+03, Con10]. Comparing the output characteristics extracted before and after degradation, Figure 4.27b and Figure 4.29b, respectively, besides the reduction of the drain current level, it is possible to observe that the adsorption of oxygen by the nanoparticle layer has caused an

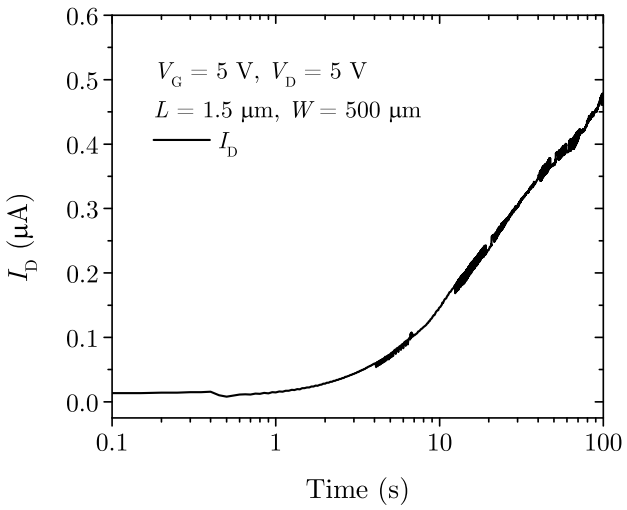


Figure 4.30: Stress test under constant bias in a ZnO nanoparticle TFT employing the high-k nanocomposite as gate dielectric.

increase on the contact resistance at the drain and source contacts. This can be explained by the formation of a depletion region induced by the oxygen trapped at the nanoparticle surface in the contact areas.

In order to investigate the oxygen desorption over time, a stress test was performed, as shown in Figure 4.30. An increase in the drain current was detected, which is in agreement with the hysteresis direction and with the increment of charge carriers in the film, as more oxygen is released from the nanoparticle surface. Besides the ascendant drain current over time, there is a discrete current fluctuation similar to the ones observed when applying PVP as gate dielectric. As discussed previously, a trap located in a particular path in the semiconductor film may reduce the current level or even block it entirely. The switching of such traps may lead to step-wise increments and reductions of the current level of a transistor at fixed drain and gate voltages.

The transistors were characterized once again after 1 month. An increased degradation over time could be detected. Nonetheless, such result was expected, since the sample was stored in a dark environment under ambient air, where the oxygen molecules could interact with the semiconducting layer for a longer period of time. Exposure to UV irradiation can be used to release the oxygen bonded at the nanoparticles surface. After exposing the sample to UV irradiation ($\lambda = 365\,\mathrm{nm}$ and $200\,\mathrm{Wcm^{-2}}$) for 60 s, it is possible to observe an increase in the drain current, which is in agreement with desorption of the oxygen and the increase of the carrier concentration in the semiconducting layer

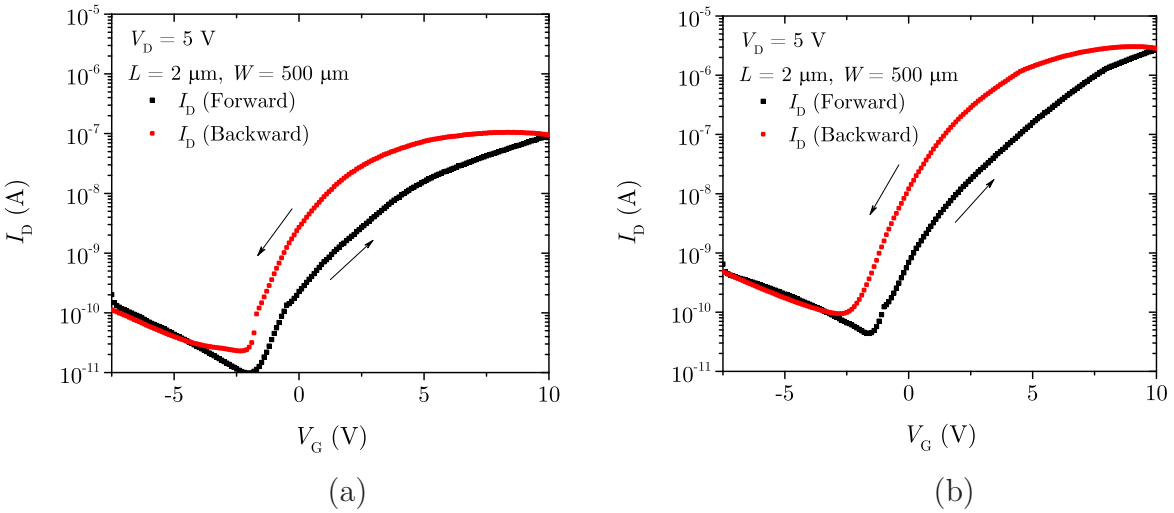


Figure 4.31: Transfer characteristics of a ZnO nanoparticle TFT after 1 month (a) pre-UV irradiation and (b) post-UV irradiation.

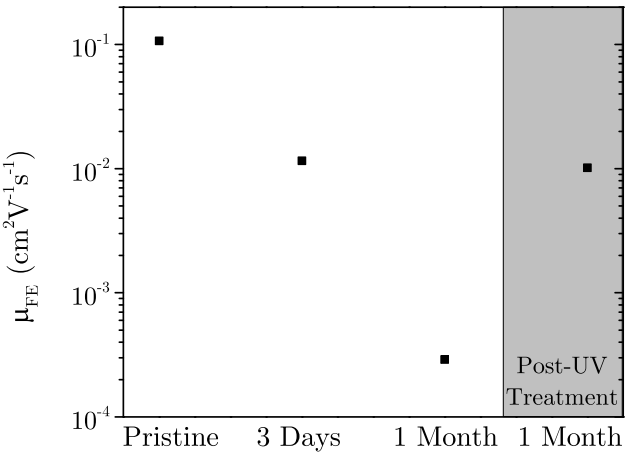


Figure 4.32: Field-effect mobility as function of time and after a UV irradiation treatment.

(Figure 4.31). Additionally, the field-effect mobility increased by almost two orders of magnitude, achieving values of around 0.01 $\mathrm{cm^2V^{-1}s^{-1}}$. Figure 4.32 depicts the variation of the field-effect mobility over time, as well as the mobility after the UV irradiation. Despite the UV treatment, the same current level and the absence of hysteresis in the transfer characteristics, which were obtained directly after the fabrication process, were not achieved again.

The substantial variation of the field-effect mobility and of the current level of the TFT pre- and post-UV irradiation further supports the hypothesis that the main mechanism responsible for the transistor degradation is the interaction between the semiconductor and the ambient air. This fact is emphasized by the large surface area of nanocompounds

and by the current flow mechanism given by percolation paths. On the other hand, the turn-on (threshold) voltage was not significantly shifted ("forward" V_{ON} from $-1.8\,V$ to $-1.5\,V$ and V_T from $1.3\,V$ to $3.8\,V$, and "backward" V_{ON} from $-1.9\,V$ to $-2.2\,V$ and V_T from $-0.9\,V$ to $1.0\,V$), which indicates that traps in the high-k dielectric and at the interface between this nanocomposite and the semiconducting layer are not the main mechanism responsible for the observed aging effect. Variations on the threshold voltage are usually related to charge trapping in the dielectric or at the semiconductor/dielectric interface and at the channel [OLS+08, CKY11, PCY12]. The turn-on (threshold) voltage values from previous studies performed in the department [6], [33], [WH09], in which thermally grown SiO_2 was used as gate dielectric, are in the same range as the ones extracted using the high-k resin. This fact also supports the assumption that traps in the semiconductor/dielectric interface are not the main cause for the instability in the fabricated TFT.

Since the main issues regarding the TFT reliability were attributed to the nanoparticulated layer, efforts were directed towards understanding the causes of the instability. For the previous transistors, the drain and source electrodes were integrated by lift-off technique on top of the active semiconducting layer (inverted staggered setup); therefore, the ZnO nanoparticles were chemically and physically stressed during the processing, inducing instabilities in the TFT operation. Another cause of reliability concerns is related to the density of defects present in the nanoparticulated material itself. In order to avoid the chemical and physical stresses endured by the ZnO nanoparticles as well as to evaluate different semiconducting compounds, the transistor setup was exchanged to inverted coplanar. This setup possesses the advantage of a "stress-free" semiconductor, as its deposition is the last step in the integration of the TFT. Furthermore, to increase the compatibility of the transistor template to polymeric substrates and to avoid the stress endured by the gate dielectric, the employment of the oxygen plasma treatment (Section 3.6.1) prior to the deposition of the high-k resin and of the nanoparticle dispersion was discontinued. Additionally, the maximum temperature used in the integration process was reduced to about $115\,℃ - 120\,℃$[21]. First experiments were performed without the structuration of the gate electrode (a continuous metal layer was used) aiming at a reduction of the integration process duration and complexity. Nevertheless, gate contacts

[21] The maximum process temperature depends on the photoresist Clariant AZ 5214E that can be employed using its positive (115 ℃) or negative (120 ℃) tone character as described in [Mic00].

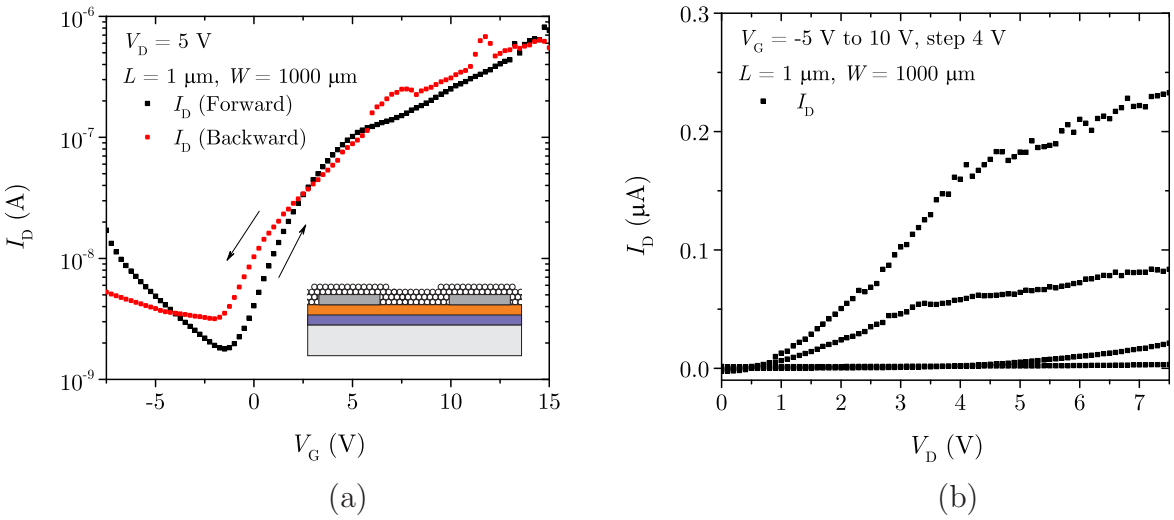


Figure 4.33: Transfer (a) and output (b) characteristics of an inverted coplanar TFT with spin-coated ZnO nanoparticles provided by Nanophase Cooperation Inc. The inset depicts the cross-section of the TFT.

and their connections were structured once the active semiconductor depicted promising characteristics.

Taking advantage of the late semiconductor deposition, diverse nanoparticle dispersions (listed in Section 3.2.3) were evaluated and classified based on aspects such as defect density, stability over time (agglomeration and sedimentation), homogeneity and deposition quality. One of the main issues was the hydrophobic character of the gate dielectric layer after the drain and source patterning by lift-off technique. Since this effect imposes a limitation to the use of spin-coating method, no continuous semiconducting layer was found in the active channel region when applying the water-based dispersion provided by Degussa GmbH. Employing the nanoparticle dispersion provided by Nanophase Cooperation Inc. operating TFTs were characterized, depicting promising aspects despite the inefficient deposition quality. Figure 4.33 presents the transfer and output characteristics of one of these transistors.

In spite of the inverted coplanar setup used, the transistor depicted low operating voltages (V_{ON} near to zero), an adequate current level and modulation, and a slight saturation of the drain current in the output characteristics. Nevertheless, the yield of operating transistors as well as their performance (μ_{FE} on the order of $10^{-4}\,cm^2V^{-1}s^{-1}$) should be improved. Aiming at a better deposition quality of the nanoparticle dispersion, a spray-coating technique was used. Profiting from capillary effect, the solution was primary deposited in the active region of the transistor, increasing the number of operating tran-

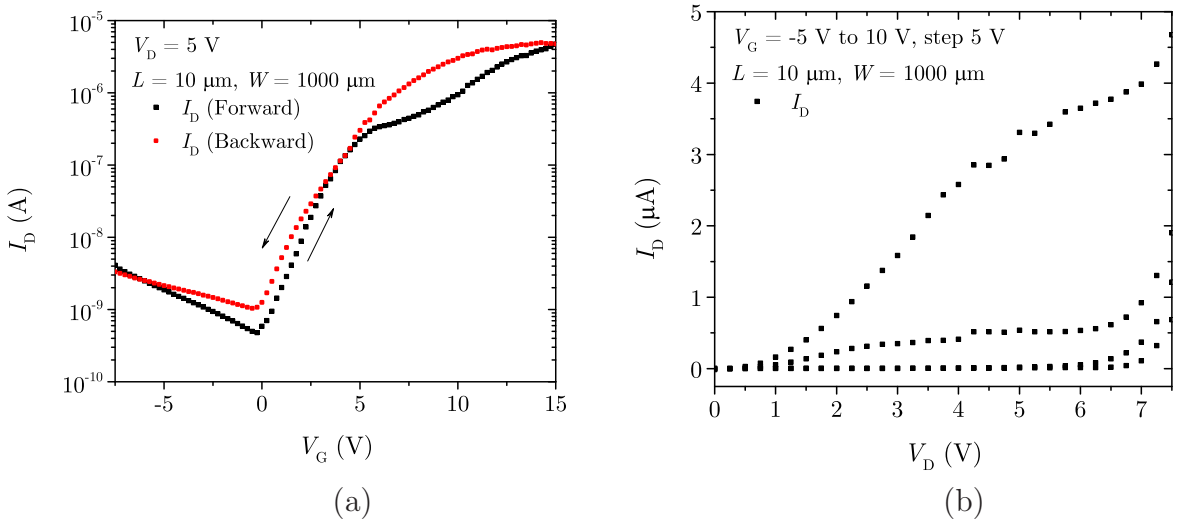


Figure 4.34: Transfer (a) and output (b) characteristics of an inverted coplanar TFT with spray-coated ZnO nanoparticles provided by Nanophase Cooperation Inc.

sistors and their electrical performance. The input and output characteristics are shown in Figure 4.34. The transistor V_{ON} is close to 0 V, the μ_{FE} is around $4 \cdot 10^{-2}\,cm^2V^{-1}s^{-1}$ (almost two orders of magnitude higher in comparison to the spin-coated device), and the I_{ON}/I_{OFF} ratio and subthreshold swing are in the range of 10^4 and 1.5 V/dec, respectively. The improvement of the electrical performance, especially the drain current level, was mainly attributed to the better contact quality between the metal electrodes and the nanoparticles due to the hydrophilic character of the aluminum-based electrodes and to the method employed for the deposition of the semiconducting dispersion.

The TFT with sprayed ZnO depicted encouraging electrical characteristics and almost no hysteretic behavior in the transfer $I - V$ curve. For comparison reasons, the ZnO nanoparticle dispersion provided from Degussa GmbH was also deposited using the spray-coating method. The transfer and output characteristics are depicted in Figure 4.35. It is possible to note a non-saturation of the drain current in the output curves as well as a hysteretic behavior in the transistor operation similar to the one observed when applying the inverted staggered setup. This effect reinforces, once again, that the application of the high-k nanocomposite as gate dielectric material is not the primary factor for the TFT instability, but rather the defects in the ZnO nanoparticles. During the selection of the nanoparticle dispersion (Section 3.2.3), the PL spectra were analyzed in order to evaluate the intrinsic density of defects present in the ZnO nanostructures. By a direct comparison of both dispersions (Figure 4.36), it is possible to see a clear difference between

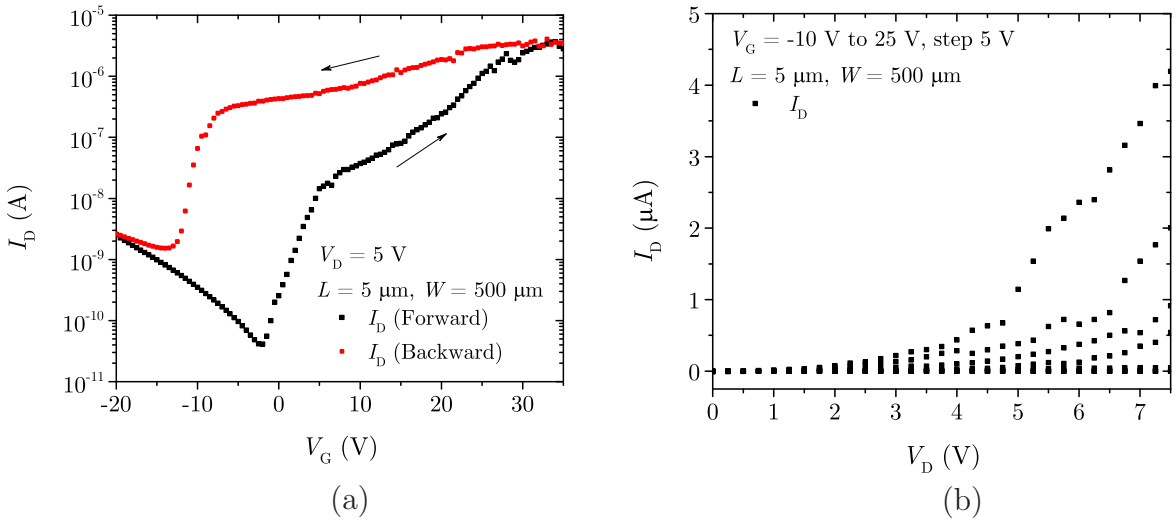


Figure 4.35: Transfer (a) and output (b) characteristics of an inverted coplanar TFT with spray-coated ZnO nanoparticles provided by Degussa GmbH.

their NBE/DLE ratios, which strongly indicates that the prior transistor reliability issues are related to the active semiconducting layer.

In order to improve the deposition quality of the aqueous solution containing the nanoparticles[22], as well as the yield of operating transistors, the spray-coating process was performed on both heated and oxygen plasma treated templates. Such procedures aimed at the increase of the template's wetting properties[23]. By heating up the template to 60 ℃ – 80 ℃ before the application of the nanoparticle dispersion, there are simultaneous deposition and evaporation of the solution during the spray-coating process. Although this procedure has increased transistor yield, formation of large grain boundaries and agglomeration of nanoparticles occurred, as already shown in Section 2.1. Analogous to the use of large nanoparticles, as described by [OMNH08, OH10], these large grains lead to accumulation and trapping of charge carriers, inducing to a hysteretic behavior in the transistor transfer characteristics (Figure 4.37a). Besides the slight increase of the TFT instability, the V_{ON} was not drastically influenced; it is still around 0 V. On the other hand, the μ_{FE} is reduced from $4 \cdot 10^{-2}\,cm^2V^{-1}s^{-1}$ to $7 \cdot 10^{-3}\,cm^2V^{-1}s^{-1}$ in comparison to the results of the spray-coating process performed on a template at room temperature. Another

[22] The nanoparticle dispersion provided from the Nanophase Corporation Inc. is the main semiconducting material from this point on. In the case of the employment of another dispersion, for the specific case it is discussed in the text.

[23] The results concerning the investigation of the electrical characteristics of the TFT using oxygen plasma treatment prior to the deposition of the nanoparticles by spray-coating technique or heating up the wafer during the spray process were partially published in [26].

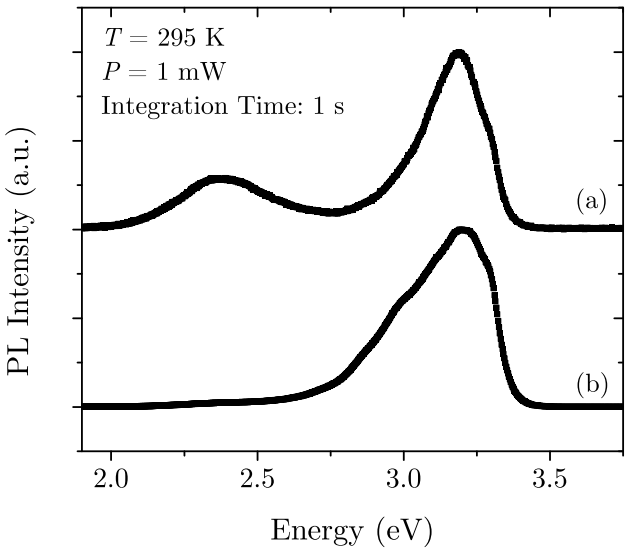


Figure 4.36: Direct comparison between the PL spectra of the ZnO nanoparticles provide by (a) Degussa GmbH and (b) Nanophase Corporation Inc.

aspect observed is a higher current in the transistor off-state; this can be ascribed to the semiconducting film thickness (which, in this case, is thicker) [BPM$^+$06, CKY11, CLK$^+$08] and to the increase of the leakage current due to the formation of a continuous ZnO film (fringing current). By employing a treatment in O_2 plasma, the wetting properties of the template can be improved (hydrophilic surface), which has positive effect when depositing aqueous solutions. Nevertheless, this approach has some issues: (I) the O_2 plasma treatment is not entirely appropriated for polymeric substrates, (II) the aluminum drain and source electrodes are oxidized during the treatment jeopardizing the contact quality to the semiconductor, and (III) depending on the exposure duration and plasma intensity, damage of the gate dielectric is possible. The transfer characteristics of a TFT whose template was treated in O_2 plasma prior to the deposition of the nanoparticle dispersion are shown in Figure 4.37b. In comparison to the untreated transistor, it is possible to observe a decrease of the transistor current level, which is attributed to the parasitic aluminum oxide at the drain and source contacts. The V_{ON} and the S are constant, and the μ_{FE} and the I_{ON}/I_{OFF} ratio are reduced in almost two order of magnitude. Additionally, the constancy of the TFT switching point and low gate leakage current indicate that the plasma treatment has not significantly damaged the gate dielectric layer.

The density of defects in the ZnO nanoparticles plays an important role in the instability of the TFT; however, the interaction of the nanostructures with the ambient air also has a large impact on the transistor performance. Metal-oxide semiconductors are

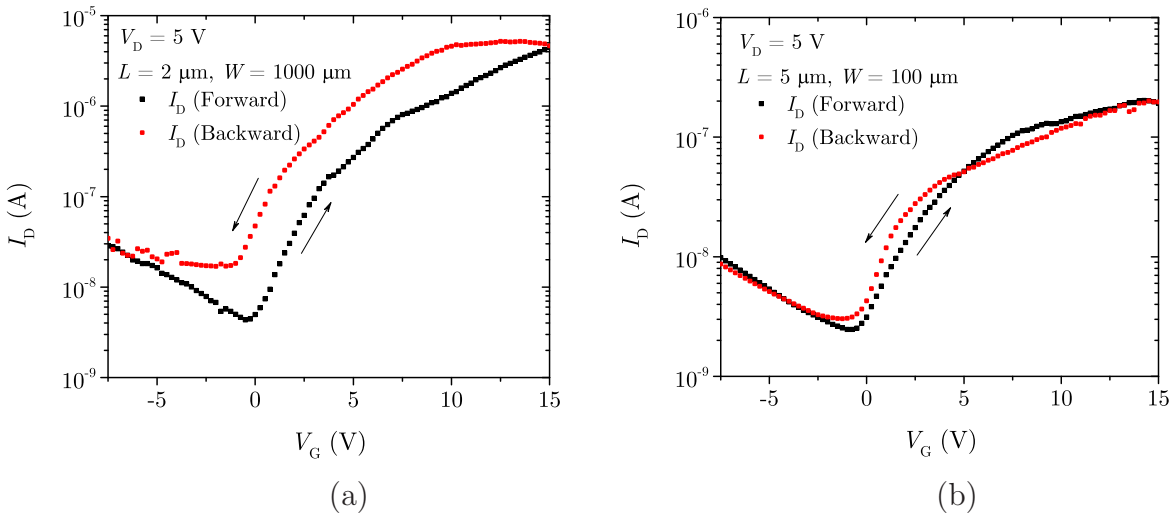


Figure 4.37: Transfer characteristics of inverted coplanar ZnO nanoparticle TFTs with deposition of the semiconductor on (a) a pre-heated template and on (b) a O_2 plasma treated template.

known to interact with molecules present in the ambient atmosphere, especially when they are used in form of nanostructures [FL05, XPST00, KM04]. For example, oxygen and water molecules have a strong impact on ZnO films, varying the charge carrier concentration and depleting the semiconductor surface [VMJ07a, Hir85, JWS+08]. On the one hand, oxygen is reported to trap free electrons [$O_2(g) + e^- \longrightarrow O_2{}^-(ad)$] at the ZnO surface, reducing the charge carrier concentration. On the other hand, water molecules partially desorb the trapped oxygen releasing electrons, hence increasing the charge carrier concentration [Mor81, LDS+09]. These effects prevent a reliable operation of the TFT. Therefore, a deeper investigation concerning the solvent vaporization step and the ZnO interaction with the ambient air was conducted[24]. Due to the high concentration of oxygen trapped at the ZnO nanoparticles surface, the pristine transistors exhibited poor electrical characteristics, as presented in Figure 4.38. For this set of transistors, structured-gate electrodes were employed, and the deposition of the nanoparticles was performed by spray-coating technique at room temperature without any prior treatment. When the transistor is stored under ambient conditions with high relative humidity (RH) ($> 50\%$), water molecules partly replace the adsorbed oxygen from the nanoparticle surface [Mor81, LDS+09]. For each oxygen released, a free electron is added to the film, increasing the drain current [VMJ07a]. Nevertheless, the adsorption of water molecules at the nanoparticle surface cannot desorb the entire oxygen content of the ZnO nanopar-

[24] The results related to this interaction and to the treatment based on UV irradiation combined with the storage in a high humidity ambient were partially published in [24].

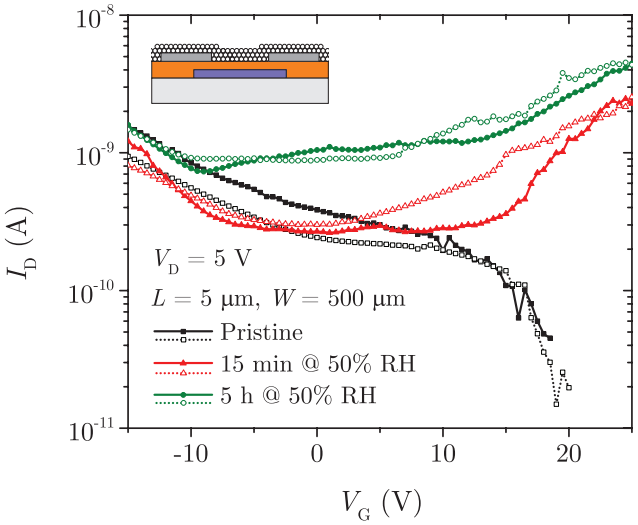


Figure 4.38: Transfer characteristics of a ZnO nanoparticle TFT showing the influence of water on the drain current. Forward sweep: solid / backward: open. The inset depicts the cross-section of the TFT.

ticle film, even when it is stored for 5 h at high RH level. Hence, the transistor will not work properly.

Aiming at a higher oxygen desorption, an UV irradiation ($\lambda = 365\,\mathrm{nm}$ and $200\,\mathrm{Wcm^{-2}}$) of 5 min was executed. In order to prevent excessive substrate heating, the treatment was done in steps of 30 s of exposure time and 30 s break, similar to the procedure already discussed for the inverted staggered setup. Upon UV illumination, electron-hole pairs are generated. These holes migrate to sites where chemisorbed oxygen is located, releasing it from the semiconducting film [JWS+08, LDS+09, PFN+16]. As a result of the reduced amount of oxygen trapped at the nanoparticle surface, the transistors show better electrical characteristics, as observed in the $I - V$ curve in Figure 4.39. The extracted turn-on voltage (V_{ON}) is in the range of $-8\,\mathrm{V}$ to $-2.5\,\mathrm{V}$, with an $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio of about 10^4 and a field-effect mobility (μ_{FE}) of $5 \cdot 10^{-4}\,\mathrm{cm^2V^{-1}s^{-1}}$. It should be noted that, as the nanoparticle surface is highly activated, oxygen and water molecules will be adsorbed/desorbed during the transistor operation. This effect may cause device instability, hence a pronounced hysteretic behavior ($\Delta V_{\mathrm{ON}} = 5.5\,\mathrm{V}$) is observed when the gate voltage is swept forward and backward. Similar results were also achieved when employing inverted staggered setup and the high-k resin, for which the UV irradiation was used after transistor aging.

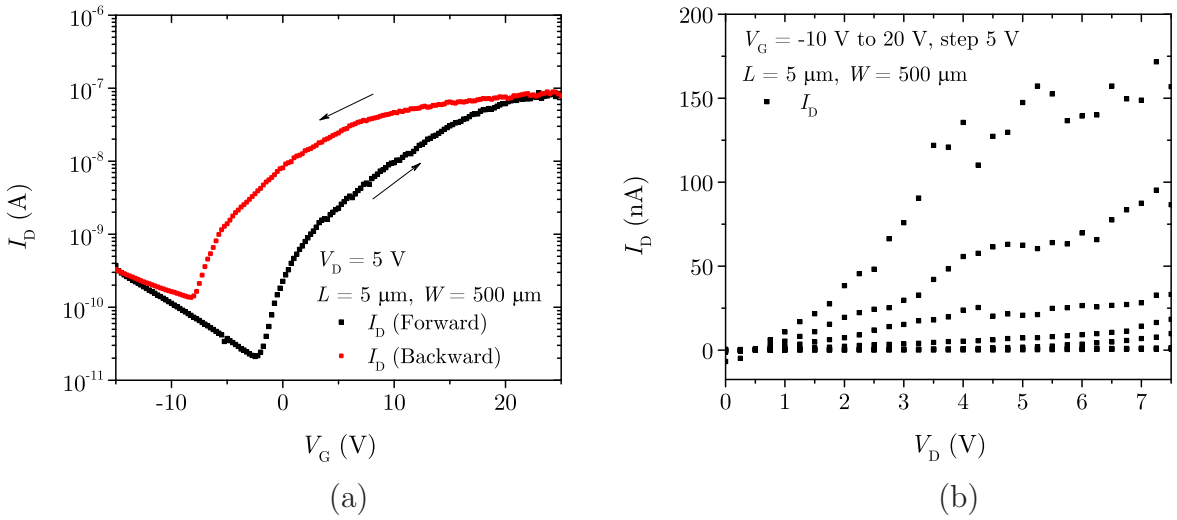


Figure 4.39: Transfer (a) and output (b) characteristics of an inverted coplanar ZnO nanoparticle TFT after UV irradiation.

The scenario when the sample is stored under high RH ($> 50\%$) conditions directly after the UV irradiation step is different; the transistors present improved and stable electrical properties with minor hysteretic behavior, as shown in Figure 4.40. The turn-on voltage is approximately $-3.5\,\mathrm{V}$, I_{ON}/I_{OFF} ratio is in the order of 10^5, and μ_{FE} is $0.1\,\mathrm{cm^2V^{-1}s^{-1}}$. The stabilization is ascribed to the physisorbed water at the nanoparticle surface that prevents the adsorption of molecular oxygen and stabilizes the semiconducting film, even when the transistors are stored and measured under ambient air with RH in the range of $25-30\%$. As a result of the variation on the RH (around 5%) during the transistor storage and characterization, the same transistor, measured 6 weeks after the UV irradiation and the high RH treatment, achieved a higher maximal drain current than in the previous measurements.

In order to understand the variation of the transistor characteristics, the qualitative model, previously discussed and presented in Figure 4.11, was adapted. Figure 4.41 illustrates the improved model, which shows the effect of oxygen and of water molecules at the nanoparticle surface subsequently to the UV irradiation exposure. As observed during the first transistor characterization, the ZnO film is saturated with oxygen molecules at the nanoparticle surface (Figure 4.41a) due to the annealing step performed in a convection oven under ambient conditions. As a result, the concentration of free electrons is low and the transistor characteristics are deficient. By adsorbing water molecules during the storage in a high humidity atmosphere, the ZnO film conductivity increases due to the addition of free electrons (released from the trapped oxygen molecules), as shown

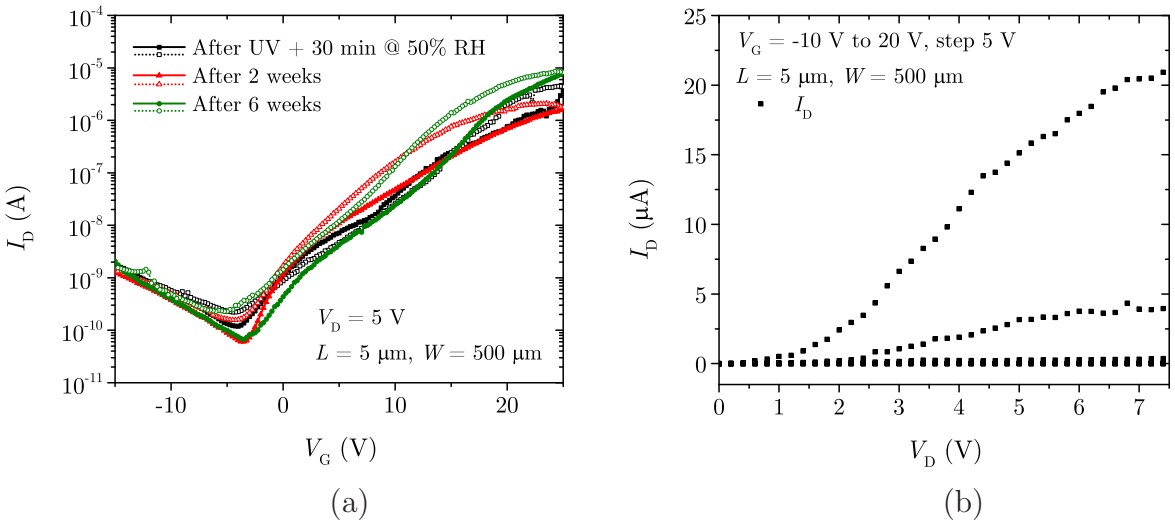


Figure 4.40: Transfer (a) and output (b) characteristics of an inverted coplanar ZnO nanoparticle TFT after UV irradiation and storage under ambient condition with high RH. Forward sweep: solid / backward: open.

in Figure 4.41b. Notwithstanding, the adsorption of water molecules saturates and the transistor will not work properly despite the increased transistor drain current level.

Since the UV illumination matches the metal-oxide band gap, electron-hole pairs are generated [JP06, ÖAL+05, FL05, JWS+08]. The holes migrate to the surface where the ionized oxygen is trapped, releasing it from the semiconductor film, as depicted in Figure 4.41c. As long as the oxygen is not adsorbed, the concentration of electrons in the film increases. Nonetheless, because of the activated ZnO nanoparticle surface, either oxygen or water molecules are again adsorbed/desorbed during the device operation; this activity creates instabilities in the device operation. This effect can be mitigated by storing the sample in a high RH environment directly after the UV illumination. After the oxygen release, the ZnO film surface is neutralized by the physisorbed water preventing oxygen adsorption (Figure 4.41d). Despite the stabilization of the nanoparticle film by the water molecules, the transistor still presents a slight hysteresis (V_{ON} = 0.5 V) in the transfer characteristics. This can be related to residual trapped oxygen, or to the existing defects in the ZnO film or at the semiconductor/gate dielectric interface. Conjointly, the discrete current fluctuations in the transistor's characteristics are attributed to trap activity at determined current paths in the ZnO nanoparticle network. Further experiments regarding the improvement of the treatment described are presented in Section 4.2.3, where a constant flow of nitrogen was used during the UV-irradiation preventing re-adsorption of oxygen molecules during the break steps.

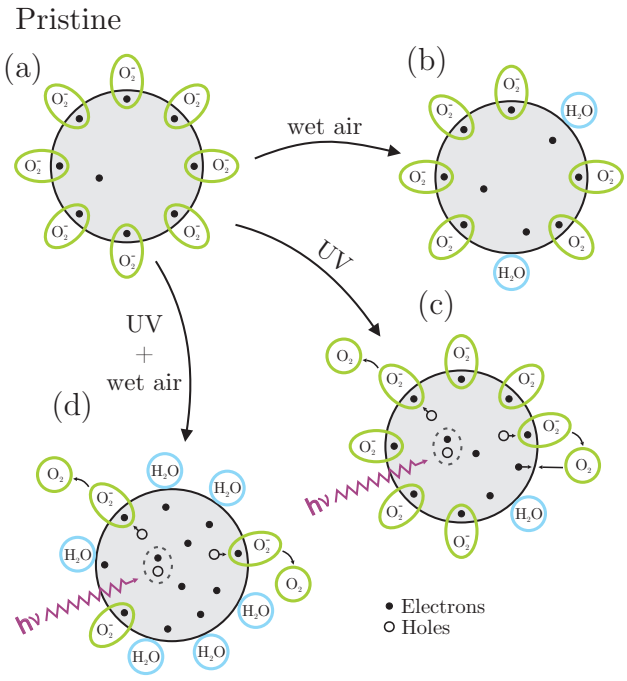


Figure 4.41: Model representing the interaction of ZnO nanoparticles with oxygen and water molecules under UV irradiation. Model based on [VMJ07a, JWS+08, LDS+09].

Based on the results concerning the stabilization of the ZnO nanoparticles provided by the Nanophase Cooperation Inc., the dispersion provided by Degussa GmbH was again evaluated in the TFT structure in order to verify the influence of this treatment on the transistor performance. Using a similar template, the dispersion was sprayed, cured and treated following the same procedure. The input and output characteristics are depicted in Figure 4.42. Due to the higher density of defects (PL spectra − Figure 4.36) of these nanoparticles, the results concerning TFT performance were different. This indicates that the nanoparticle's defect density has a strong influence on the charge carrier transport in the semiconducting material, and that the impact of the adsorbed oxygen is minor only contributing to the degradation of the TFT performance. Therefore, the use of this dispersion as active semiconductor material was not reintroduced.

As described previously in the integration section, the patterning of the drain and source electrodes by etching process leads to a hydrophilic gate dielectric surface. This characteristic increases the compatibility with the water-based dispersion containing the ZnO nanoparticles. Therefore, spin-coating technique was reintroduced in the integration process to evaluate the effect of the hydrophilic character of the template surface on the transistor characteristics. After the TFT template structuration, the semiconducting solution was spin-coated onto the sample followed by a solvent vaporization step. After the

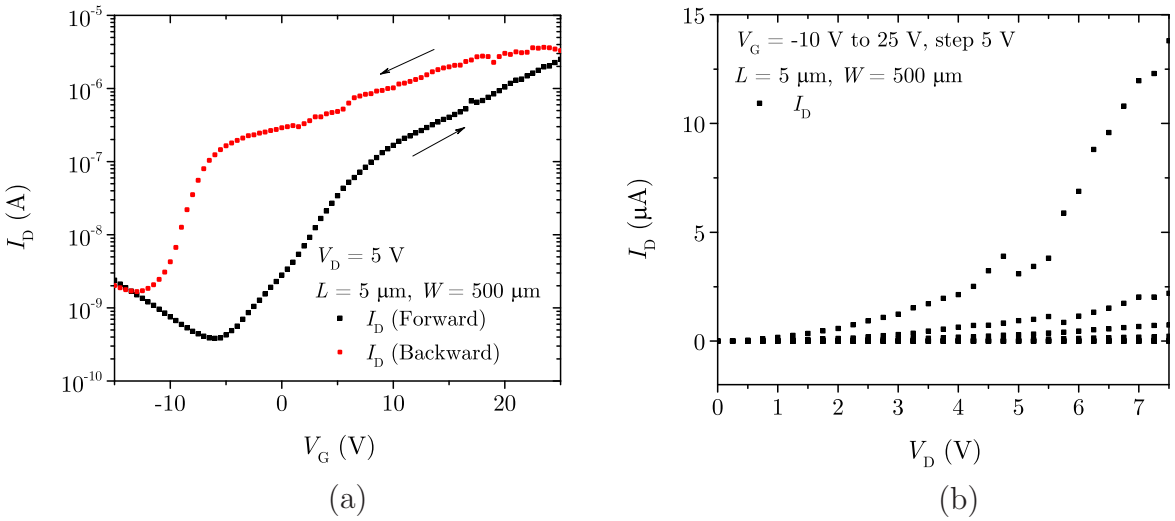


Figure 4.42: Transfer (a) and output (b) characteristics of an inverted coplanar ZnO nanoparticle TFT using the Degussa GmbH dispersion after UV irradiation and storage under ambient condition with high RH.

stabilization of the nanoparticulated film by UV irradiation combined with wet-air treatment, the transistors were electrically characterized. The transistor's transfer and output characteristics are presented in Figure 4.43. It is possible to observe a small hysteretic behavior in the transfer characteristic when the gate voltage is swept forward and backward (Figure 4.43a). This instability is related either to an incomplete stabilization of the nanoparticulated film or to the already existing defects at the dielectric/semiconductor interface, as already discussed. The TFT turn-on voltage is close to 0 V, a field-effect mobility of approximately 0.2 $cm^2V^{-1}s^{-1}$ was extracted, and the transistor depicts an I_{ON}/I_{OFF} ratio and subthreshold swing (S) in the range of 10^4 and 500 mV/dec, respectively.

Due to the reduced contact area between the drain/source electrodes and the nanoparticulated film in inverted coplanar setups, which leads to a low charge carrier injection at the contacts, the transistor current is limited. Another disadvantage of this setup is the critical definition of the spin-coating parameters during the semiconductor deposition. As the drain and source electrodes are already structured, the spin-coating process induces an uneven distribution of the semiconductor in the channel region because of the involved centrifugal forces. The decrease of the solid content in the dispersion indeed improves the deposition uniformity on the wafer, but also reduces the contact quality between neighboring nanoparticles, drastically increasing the semiconducting film resistivity. Moreover, the ZnO deposition can be improved by the use of a spray-coating technique, as prior

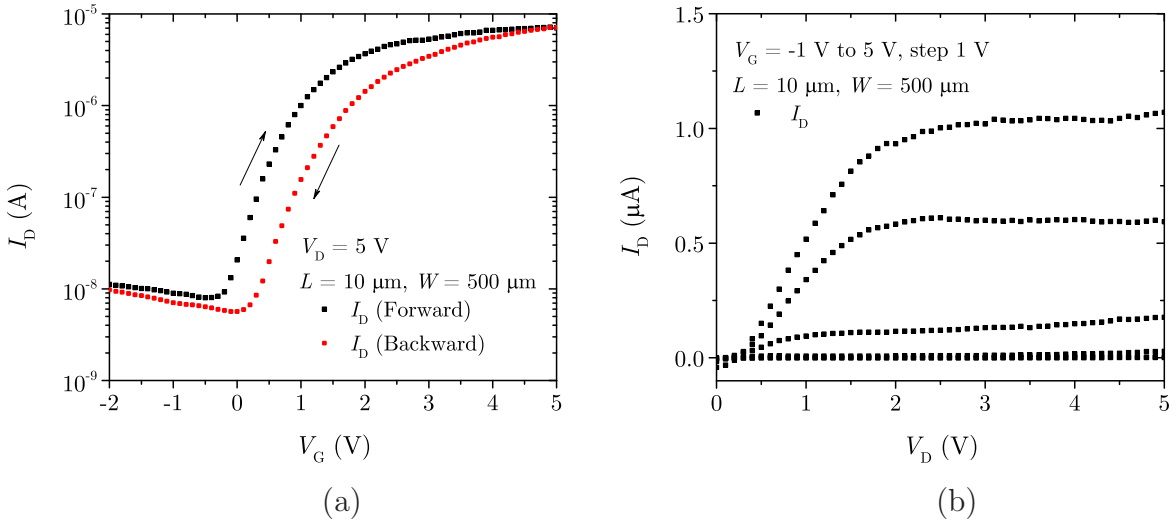


Figure 4.43: Transfer (a) and output (b) characteristics of an inverted coplanar ZnO nanoparticle TFT employing spin-coating technique for the deposition of the nanoparticle dispersion on the hydrophilic transistor template.

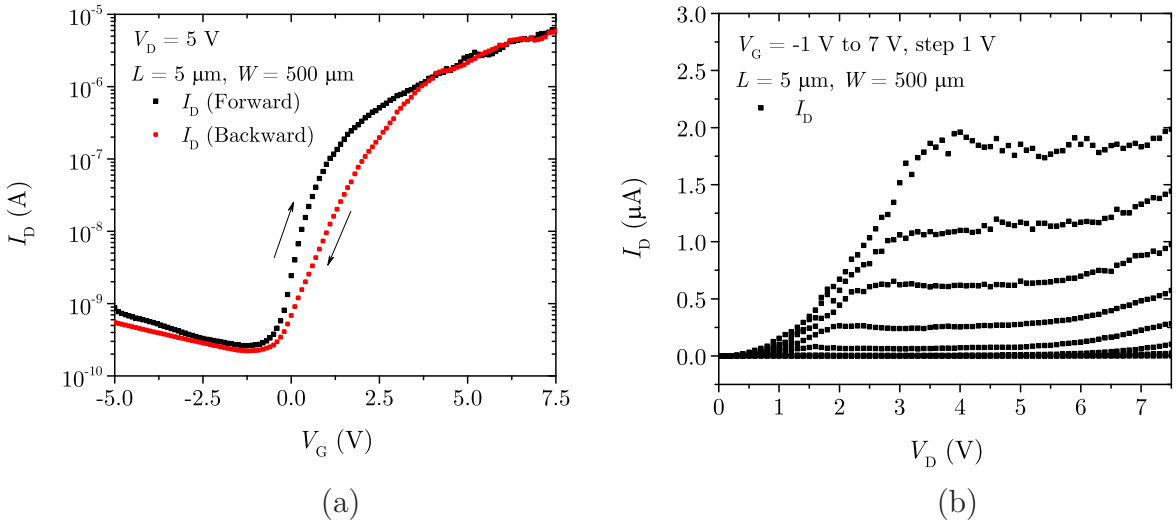


Figure 4.44: Transfer (a) and output (b) characteristics of an inverted coplanar ZnO nanoparticle TFT employing spray-coating technique for the deposition of the nanoparticle dispersion on the hydrophilic transistor template.

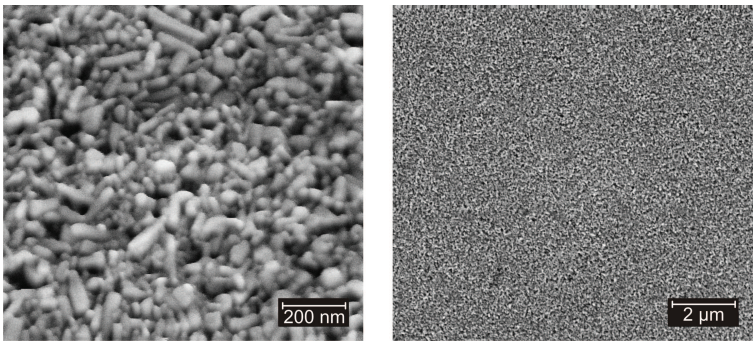


Figure 4.45: Scanning electron microscope images of the ZnO nanoparticle layer after the solvent vaporization at 115 °C in a convection oven for 1 h and the UV and high humidity treatment.

addressed. Besides the better compatibility for a large-scale production on flexible substrates, this deposition method increases the transistor performance as well as the yield of operating transistors. Figure 4.44 depicts the input and output characteristics of the TFTs employing spray-coating technique for the deposition of the nanoparticle dispersion on the hydrophilic transistor template. The μ_{FE} and the turn-on voltage have not significantly changed. An $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio and S of about 10^4 and 500 mV/dec were extracted. Scanning electron microscope images of the nanoparticulated film are shown in Figure 4.45; predominantly, spherical shaped nanoparticles with a diameter of about 70 nm are observed. This is in agreement with the dispersion specifications [Nan16c].

Based on the encouraging results achieved on rigid substrates so far, the transfer of the integration process to flexible substrates was initiated. At first, inverted coplanar transistors employing the high-k nanocomposite as gate dielectric and spray-coating technique for the deposition of the active semiconducting materials (ZnO nanoparticles) were evaluated.

4.2.3 ZnO Nanoparticle TFT on Flexible Substrates

The development of the TFT template on rigid substrate was performed aiming at a later transfer to flexible substrates. Thus, all processes steps were chosen and adjusted to be compatible with polymeric foils. Based on the improved deposition quality of the nanoparticle dispersion achieved employing spray-coating technique on the hydrophilic gate dielectric after the structuration of the drain and source electrodes by wet-etching,

this approach was chosen to be implemented on a PET substrate[25]. Despite the hindrances concerning the integration on flexible templates, the transistors depicted similar electrical characteristics when compared to their rigid-substrate counterparts. Figure 4.46 depicts the transfer and output characteristics of the ZnO TFTs integrated on a freestanding polymeric substrate. A turn-on (V_{ON}) voltage of around 1 V, a field-effect mobility (μ_{FE}) in the order of $0.5\,\mathrm{cm^2V^{-1}s^{-1}}$, an $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio of 10^5 and a subthreshold swing (S) of 500 mV/dec were extracted. An interesting aspect of this integration process is that even applying different deposition methods for the active semiconductor and using either an oxidized Si wafer or a polymeric substrate, the transistor characteristics present no significant variation. This stability depicts the robustness of the developed integration process. Nonetheless, since low temperatures (maximum temperature of 115 ℃) are used, no sintering of the nanoparticles occurs. The sintering of ZnO nanoparticulated films starts at temperatures above 400 ℃ and is reported to improve the nanoparticle interconnections [LJJ+08]. Unfortunately, higher temperatures are not applicable to polymeric substrates, unavailing such approaches. Another procedure for a punctual annealing of the nanoparticulated film is the employment of pulsed laser exposure. With this technique, the characteristic of the semiconductor can be optimized by controlling the parameter of the laser processing or the annealing ambient conditions [PMK+09, LPK+12]. Even though the annealing of the film is superficial, damaging of the semiconductor film [LPK+12] or of the gate dielectric caused by excessive laser exposure may lead to instabilities in the transistor operation. Notably, the devices of this study, however, depict performance for digital circuits without any additional sintering treatment. Furthermore, their characteristics are comparable to transistors integrated using much higher temperatures and vacuum processes, as sputtering techniques for the gate dielectric or the active semiconductor deposition [FBM12, PMV+16, LJJ+08].

The optical characteristics of the fabricated TFTs were also investigated. Figure 4.47 shows the optical transmittance measured by ultraviolet-visible (UV−Vis) spectroscopy. A transmittance of around 75% is achieved in the visible light spectrum. Due to the use of metals for the gate, drain and source contacts, the transmittance is reduced depending on the density of these electrodes. The low transparency between the wavelengths of 350 nm and 400 nm is associated to the light absorption caused by the ZnO nanoparticles. The energy levels in the band gap originated by defects in the nanoparticles lead to a

[25] The results related to the transferring process of the integration of ZnO TFT from rigid to polymeric substrates, especially the resolutions achieved in the photolithography on PET substrates were partially published in [5].

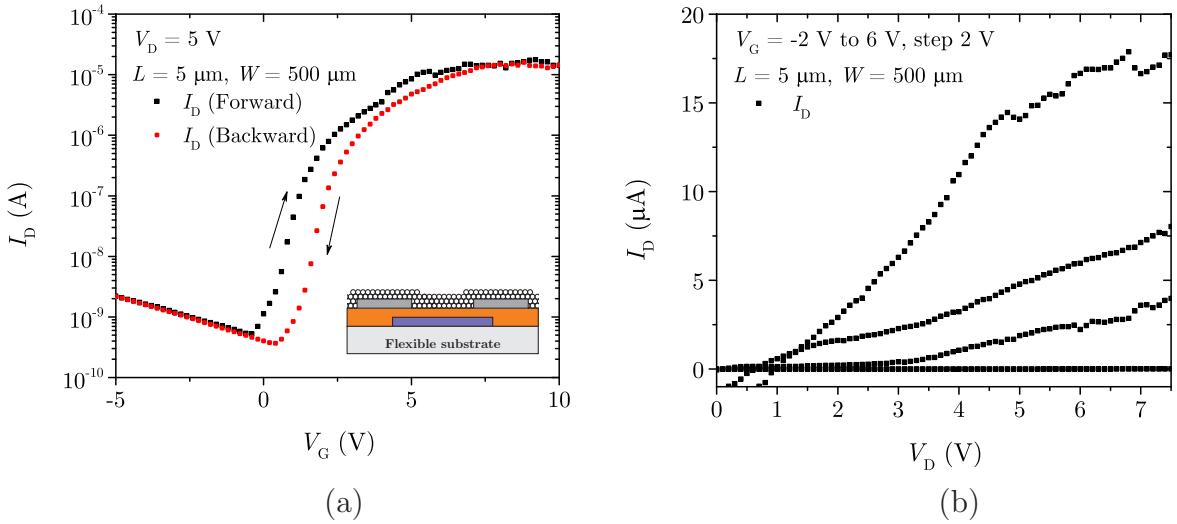


Figure 4.46: Transfer (a) and output (b) characteristics of an inverted coplanar ZnO nanoparticle TFT on a freestanding PET substrate. The inset depicts the cross-section of the TFT.

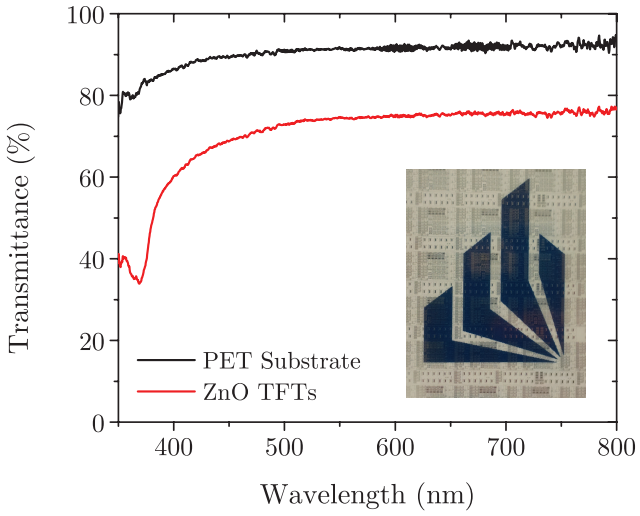


Figure 4.47: Optical transmittance of the ZnO nanoparticle TFTs on a PET substrate in the visible light spectrum. The inset shows a section of the PET substrate with the integrated transistors.

broadening of the absorption spectrum. Notwithstanding, the integrated TFTs preserve the transparency and the flexibility of the substrate, although the metal electrodes can be clearly seen, as depicted in the inset of Figure 4.47.

The partial re-adsorption of oxygen molecules during the UV exposure and wet-air treatment could lead to an incomplete stabilization of the semiconducting film. Aiming at the improvement of this process, the UV irradiation and the high humidity treatment were performed under inert gas conditions[26]. In this case, a constant flow of nitrogen removes the ambient oxygen as well as the molecules desorbed from the nanoparticles during the UV exposure step out of the irradiation chamber. For the subsequent high humidity treatment, wet-nitrogen was used.

After the treatment in N_2 atmosphere, the transistors were exposed to ambient air for the electrical characterization. The transfer $I - V$ curve is presented in Figure 4.48b. The transfer characteristics of the previous TFT treated in ambient air are shown for comparison (Figure 4.48a). An increase in the transistors instability was observed, as well as a discrete fluctuation in the drain current. The step-like fluctuations were already reported during the stress test of the transistors (Section 4.2.1). The increase of the trap influence is ascribed to the variation of the ozone amount during the UV irradiation step. The ozone is formed from the atmospheric oxygen or the molecules desorbed from the nanoparticle surface by the UV irradiation. The interaction between ozone and ZnO nanowires was already investigated and an improvement in the TFT performance was reported in [JLY+07]. On the one hand, the N_2-flow purges the released oxygen from the ZnO film and prevents its re-adsorption; on the other hand, the ozone is also removed from the reaction chamber, and so it is unable to react with the semiconducting film.

As reported by Martin *et al.* [MFN+04] and Goncalves *et al.* [GPF+06], ozone reacts with the defects at the grain boundaries of sputtered ZnO, acting as a donor element and increasing the conductivity and connectivity between grains. Analogously, this effect can be applied to the ZnO nanoparticles. During the synthesis of the nanostructures, the majority of defects are concentrated at the surface of the compound [JP06, Kli07, FL05]. Traps at the connections between neighboring nanoparticles have a major influence on the charge carrier flow through the nanoparticulated film as already anticipated when a step-like behavior was observed in stress test at constant bias. Consequently, the traps at

[26] The results related to the UV exposure combined with high humidity treatment under inert atmosphere were partially published in [19].

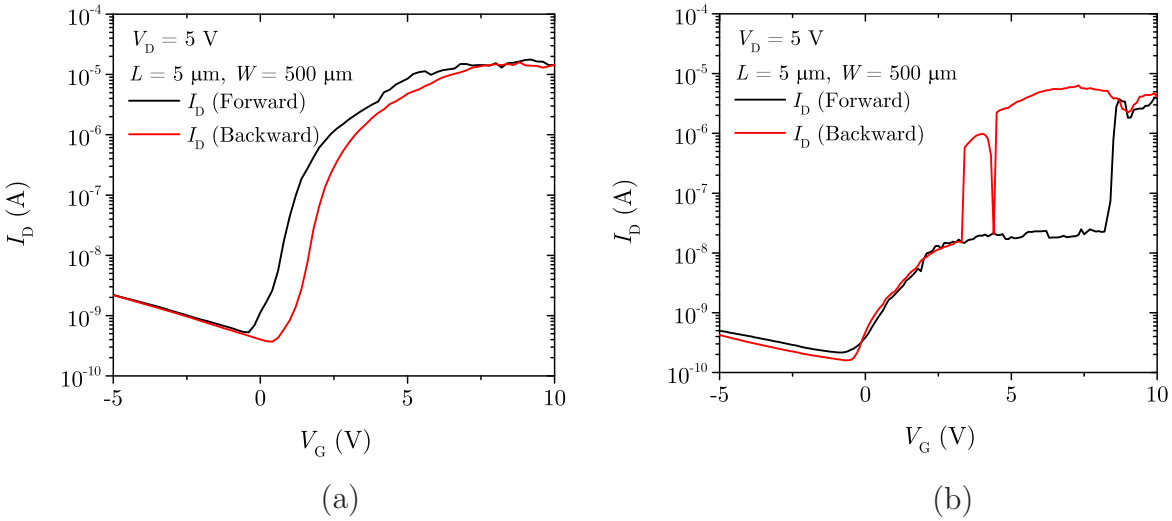


Figure 4.48: Transistor transfer characteristics (a) after the UV irradiation step combined with a wet-air treatment and (b) with a pure nitrogen flow during the treatment.

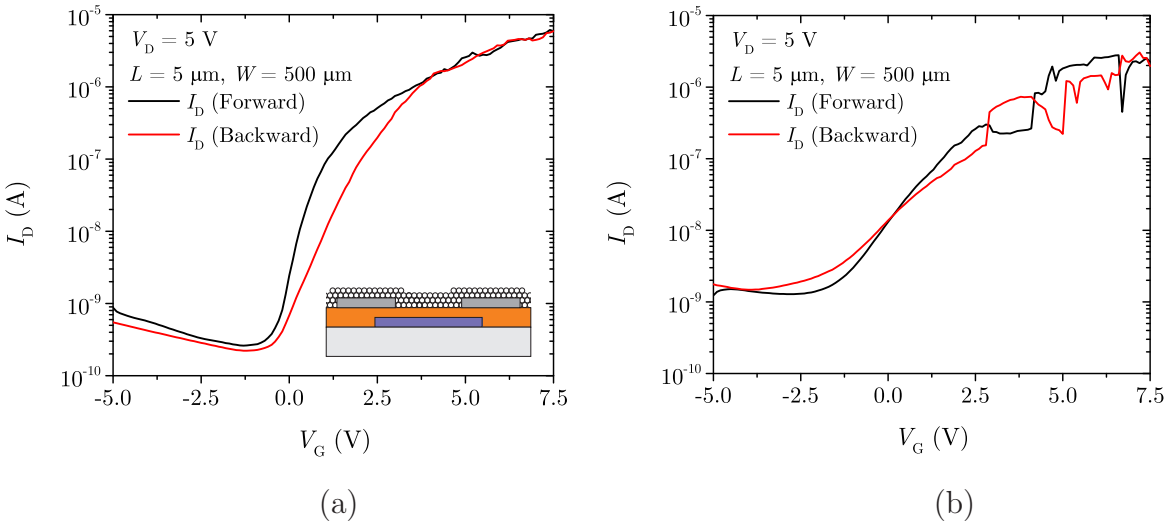


Figure 4.49: Transfer characteristics of ZnO TFTs on rigid (Si-based) substrate (a) after the UV irradiation step combined with a wet-air treatment and (b) with a pure nitrogen flow during the treatment.

ZnO nanoparticles can be categorized in two groups: one related to the adsorbed oxygen molecules, which reduce the charge carrier concentration jeopardizing the current flow magnitude, and the other related to defects in the ZnO structure, which interact with the ozone produced during the UV irradiation step. By intense UV exposure under ambient conditions, the majority of the oxygen at the nanoparticle surface is released increasing the charge carrier concentration in the ZnO film. Conjointly, the interaction between the ozone and the ZnO crystal defects increases the connectivity of neighboring nanoparticles [MFN$^+$04].

In order to confirm that the increase on the transistor instability is not directly related to the polymeric substrate and its mechanical flexibility, the same procedure was performed on a rigid template. As it is possible to observe in Figure 4.49, a similar effect was noted in TFTs integrated on an oxidized Si wafer. Therefore, the increase of the instability can be ascribed to the reduction of the ozone amount in the treatment, and it is not related to the flexible template itself. Conjointly with the investigation of the semiconductor stabilization under inert gas, other variations of the treatment were also investigated. By placing the sample at the exhaust system of the UV-lamp (the concentration of ozone is high and the UV irradiation is minimized), the sample depicted deficient electrical characteristics, which is in agreement with the oxygen bounded to the ZnO nanoparticles trapping charge carriers. Increasing the relative humidity during the exposure, *i.e.* the UV irradiation is performed at a constant wet-air flow, the transistor presented a strong turn-on voltage shift. This effect is related to the additional influence of OH^- groups at the surface during the UV irradiation. By performing this test under inert gas atmosphere (constant flow of wet-N_2), a shift of V_{ON} similar to the previous test as well as deterioration of the subthreshold swing were observed. These effects are also attributed to the reduced amount of ozone in the chamber during the treatment. The respective transfer curves of the TFTs are shown in Figure 4.50. It is known that a deeper investigation concerning different atmospheres, humidity levels as well as the evaluation of stabilization mediums as alcohol vapors, *e.g.* ethanol, isopropanol or acetone, instead of a high humidity environment should be performed. However, based on the results obtained up to this point, the transistors treated under ambient air were the ones that depicted better electrical performance and stability.

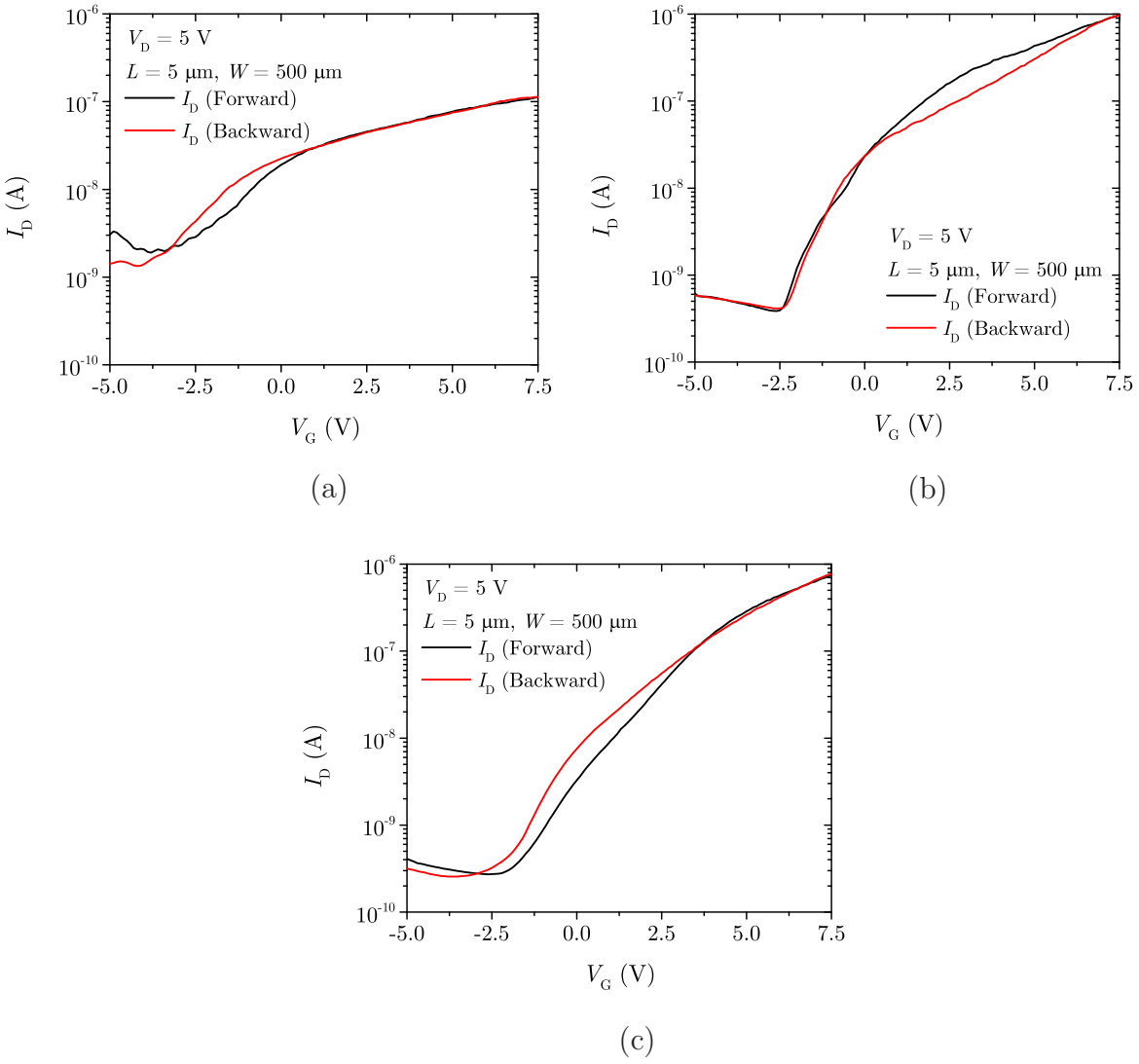


Figure 4.50: Transfer characteristics of ZnO TFTs on rigid substrate (oxidized Si wafer) treated with (a) ozone, (b) UV and high humidity simultaneously and (c) UV and high humidity simultaneously under inert atmosphere.

4.3 Performance Improvement: Application of Inverted Staggered Setup

As already discussed throughout this study, especially in Section 3.1, the main drawback of inverted coplanar setups is the poor contact quality between the drain and source materials and the semiconducting film. Whereas, by applying an inverted staggered setup, the drain and source electrodes are structured on top of the semiconducting layer, hence a better contact quality can be achieved.

With the employment of inverted coplanar structures to improve the transistor reliability as well as compatibility to polymeric substrates, the main instability mechanisms in the ZnO nanoparticles TFTs could be identified and minimized without a substantial increase in the production costs. Afterwards, in order to improve the performance of the elementary transistor, an inverted staggered setup can be applied. Considering the integration aspect, one drawback of this setup is the chemical stress suffered by the semiconducting layer during the structuration of the drain and source electrodes. Many research groups avoid this stress by using a shadow mask technique for the deposition of the electrode material; however, this method impedes the integration of compact circuits and is not entirely suitable for large-scale production. Hence, conventional contact photolithography technique and a lift-off process were used for the definition of the drain and source areas. To avoid the processes instabilities related to the polymeric substrate, first experiments were performed on rigid substrates (oxidized Si or glass wafers) and later transferred to freestanding flexible templates.

For the integration of this transistor setup, the processes up to the gate dielectric deposition and curing/cross-linking step are the same as the ones followed for the inverted coplanar. After the achievement of a hydrophilic character of the gate dielectric layer surface through a chemical activation, as described in Section 3.6.1, the nanoparticle dispersion is deposited. As no structures (drain and source electrodes) were present at this point on the sample, spin-coating technique was used. The application of the spray-coating method is also possible; however, the deposition of a layer with an even thickness on large area samples is complicated with the current deposition setup available in the Sensor Technology Department of the Paderborn University. Afterwards, via connections through the semiconducting layer and the gate dielectric were opened using photolithography and wet-etching techniques to contact the gate electrode. Finally, the drain and

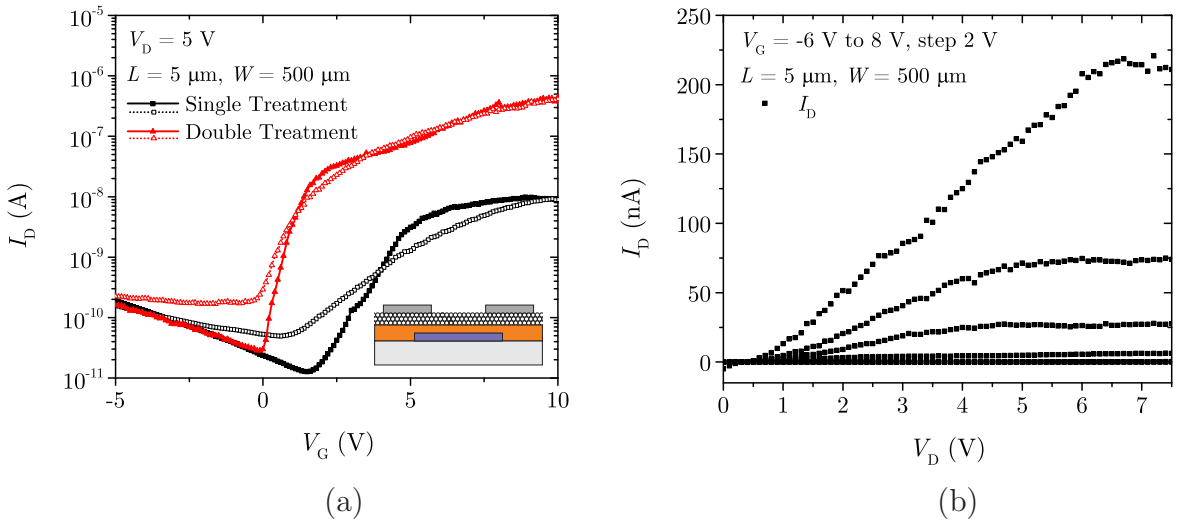


Figure 4.51: Transfer characteristics (a) of an inverted staggered ZnO nanoparticle TFT with the stabilization of the semiconducting layer after the integration process. Output characteristics (b) of the double treated transistor. Forward sweep: solid / backward: open. The inset depicts the cross-section of the TFT.

source electrodes were structured by lift-off technique of a 150-nm thick aluminum layer evaporated under high-vacuum conditions.

Subsequent to the transistor integration, the UV irradiation and wet-air treatment were performed as described for the inverted coplanar setup[27]. The transistor transfer characteristics of the inverted staggered setup device are shown in Figure 4.51. Due to the shadowing effect originated by the drain and source material (non-transparent), the area of the semiconducting layer underneath the electrodes was not directly affected by the UV irradiation. However, as a result of scattering centers present in the nanoparticulated film and of the porosity of the layer, the ZnO nanoparticles under the drain and source contacts could be partially exposed to the stabilization process. The presence of organic residues (photoresist) from the photolithography may also deteriorate the effectiveness of the stabilization treatment. These residues can be removed by intense UV irradiation and ozone exposure [Vig85, KH16]. Therefore, a second treatment step was carried out in order to increase the exposed ZnO section and to remove possible organic contaminations. The electrical characteristics after the double stabilization process are depicted also in Figure 4.51. No further improvement of the transistor characteristics were ob-

[27] The results related to stabilization of the ZnO nanoparticles in inverted staggered TFTs were partially published in [12].

served by executing additional treatment sequences since the channel section of the active semiconducting layer was overexposed to UV-irradiation.

Aiming at an even stabilization of the nanoparticulated film, the treatment in the integration process order was shifted: instead of being the last step, it was placed prior to the structuration of the drain and source electrodes. Moreover, the semiconducting layer stabilization may act as a protection (due to the physisorbed water molecules) preventing the adhesion of organic residues from the photolithographic step. The expected performance improvement when the inverted staggered setup is applied[28] can be noted by the transistor transfer and output characteristics shown in Figure 4.52. The field-effect mobility has increased from about $0.2\,\mathrm{cm^2V^{-1}s^{-1}}$ to $3.7\,\mathrm{cm^2V^{-1}s^{-1}}$ and the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ from 10^4 to 10^7 compared to the spin-coated inverted coplanar TFT. The subthreshold swing has also improved significantly, and it reaches values of about 130 mV/dec. The turn-on voltage is about 0.5 V and has not significantly changed in comparison to the prior integrated transistors either using spin-coating or spray-coating deposition techniques. From the $I-V$ curves of the transistor, it is possible to note that the on-state current level is about two orders of magnitude higher, which is attributed to the better charge carrier transport through the drain and source contacts due to larger contact area. Moreover, the off-state current reduction is ascribed to the semiconducting layer region between the overlapped area of the drain/source and gate electrodes prior to the channel formation ($V_{\mathrm{G}} < V_{\mathrm{ON}}$). This effect leads to an access resistance, typical from inverted staggered setups, hence reducing the leakage currents in the transistor when negative gate voltages are applied. Further improvement can be observed by the drain current slope (drain conductance $-\delta I_{\mathrm{D}}/\delta V_{\mathrm{D}}$) in the linear region of the output characteristics. Since the UV and high humidity treatment was performed before the drain and source electrodes integration, no shadowing effect occurs and the charge carrier injection in the transistor channel is improved. Since the treatment endured the photolithographic process without a significant decrease in its effectiveness, this outcome was ascribed to a double layer surface formation [Lan32]. As a consequence of the large surface area present in the nanoparticulated film and of the low-temperature processes used during the TFT integration, the treated ZnO surface is able to endure the upcoming processing steps.

The improved transistor performance is ascribed to the better contact quality due to the increased contact surface between the drain and source electrodes and the nanopar-

[28] The results related to the comparison of the inverted staggered TFT with the inverted coplanar counterpart were partially published in [4].

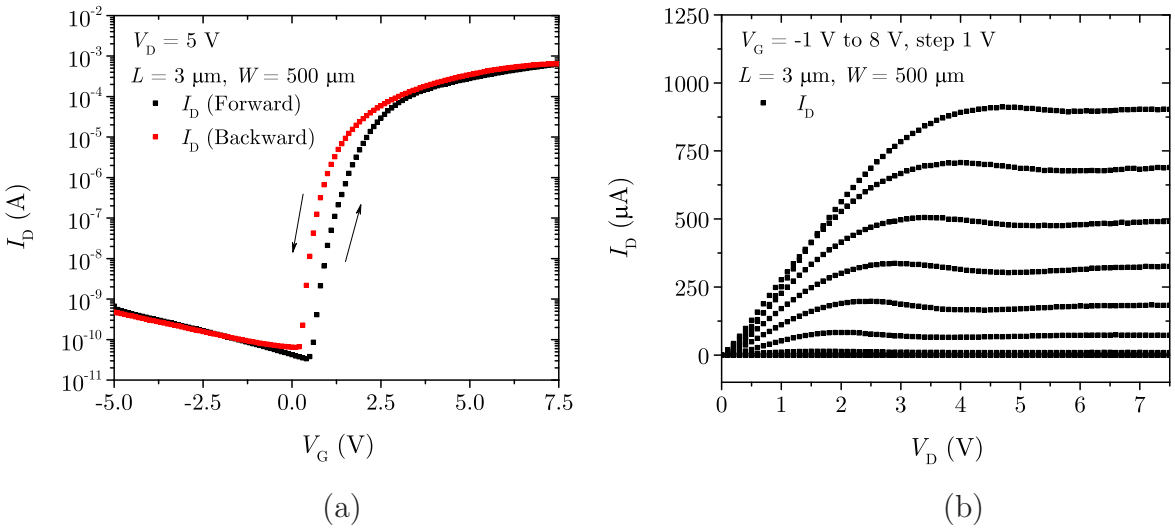


Figure 4.52: Transfer (a) and output (b) characteristics of a ZnO nanoparticle TFT on oxidized Si wafer applying an inverted staggered setup.

ticulated film. However, a precise and reliable estimation of the contact resistance value and of the mechanism responsible for the charge carrier injection are still under investigation. The hindrances are related to the semiconducting film morphology. As the current transport in the ZnO nanoparticles is based on percolation paths, discrepancies in the estimation of the resistance values are induced by this characteristic. Additionally, as the metal-semiconductor contacts are influenced by the applied bias, a non-linear and non-ideal behavior is also commonly observed [VMJ07a]. Studies reporting on the conduction mechanisms in non-crystalline ZnO films can be found elsewhere [Meu99, MBF+07]. The current transport is strongly affected by the film defect density and grain boundaries. When using ZnO nanowires, for instance, their orientation and network formation are even more critical, as the electrostatic coupling between the semiconducting material and the gate electrode is poor, requiring higher gate voltages for the device operation [KPP+08, KHL+13].

To the best of our knowledge, the transistor metrics extracted for the inverted staggered setup are among the best reported for ZnO nanoparticle TFTs. In comparison with the results presented in this study, Faber *et al.* have described TFTs depicting higher charge carrier mobilities; however, they show a highly pronounced hysteresis in the transfer characteristic [FHK+12]. For an improvement of the performance, the ZnO nanoparticles were treated in oxygen plasma [FHK+12]. This approach induces instabilities in the transistor operation and prevents its integration on flexible substrates as the oxygen plasma damages the template as well as polymeric dielectrics. Cho *et al.* have reported ZnO-based

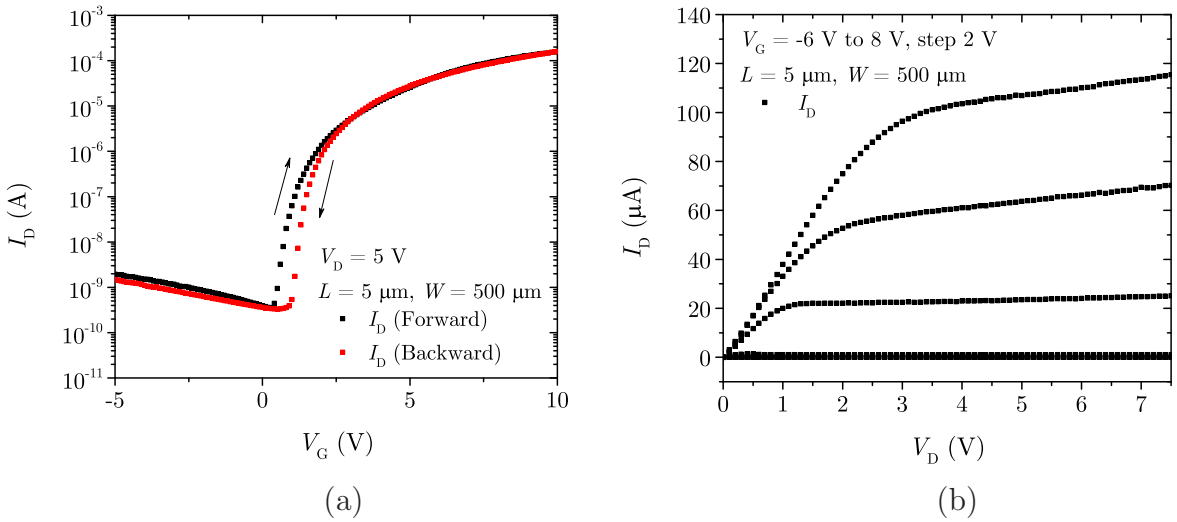


Figure 4.53: Transfer (a) and output (b) characteristics of a ZnO nanoparticle TFT on borosilicate glass substrate applying an inverted staggered setup.

TFTs integrated using a nanoparticles and precursor mixture ink in order to achieve a better film morphology enhancing the transistor performance [CKJ+12]. Nevertheless, for the formation of the semiconducting film, temperatures of 250 ℃ are required, limiting the compatibility of the integration process to certain polymeric substrates or to glass. TFTs with similar characteristics were also discussed by Park *et al.*, in which alkali metal doped ZnO was applied as the active semiconductor, requiring higher temperature processing, too [PKK+12]. The electrical characteristics are also comparable to the ones of TFTs with semiconductors fabricated employing ZnO precursors, however high temperatures or annealing under strict atmosphere are essential to reduce instabilities and to assure operation at low voltages [MAH+08, TBS+11]. ZnO-based TFTs using sputtering techniques depict denser semiconducting films besides the possibility to vary the semiconductor composition by adding In, Ga or Sn, for example. Such TFTs usually present higher performance [BPG+09, FPP+04, LKKP07]. Notwithstanding, the transistors reported in this study present similar metrics using low-cost fabrication processes and materials, as well as integration steps that are fully compatible to flexible substrates.

Employing a different rigid substrate, *i.e.* borosilicate glass wafer, the TFT electrical characteristics have suffered minor variations. The transfer and output $I-V$ graphs are shown in Figure 4.53. A turn-on voltage of approximately 0.5 V, a field-effect mobility of around $1-3\,\mathrm{cm^2V^{-1}s^{-1}}$, a subthreshold swing of about 250 mV/dec and I_{ON}/I_{OFF} in the range of 10^6 were extracted. The main difference in the processing is the relative critical photoresist developing step prior to the lift-off technique, in which organic residues could

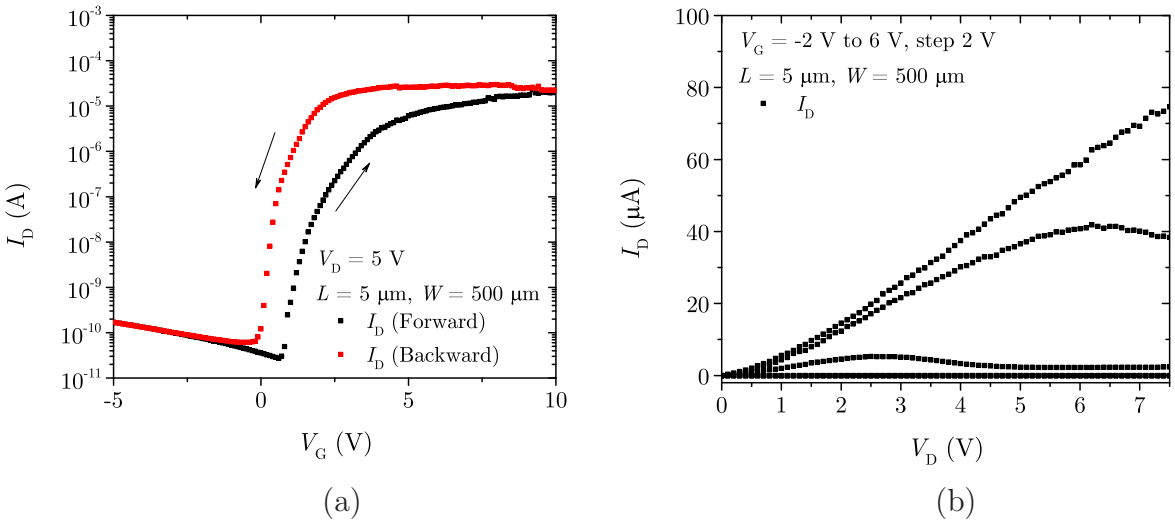


Figure 4.54: Transfer (a) and output (b) characteristics of a ZnO nanoparticle TFT on borosilicate glass substrate applying an inverted staggered setup after degradation over time.

be present, causing variations in the contact quality. Overdevelopment of the photoresist may damage the gate dielectric underneath the semiconducting layer. This issue is critical for flexible substrates, as described later in this section.

Even considering the double layer surface at the nanoparticles, the stabilization of the semiconducting layer can be jeopardized due to the strong alkaline solution applied for the development process, and to the use of solvents during the lift-off process for the structuration of the drain and source electrodes. Hence, when storing the sample in a low humidity atmosphere (less than 30% RH), a slight aging effect was noted. This can be observed by the comparison between the original characterization (Figure 4.53) and the one performed after a couple of days (Figure 4.54). The right shift of the turn-on voltage, the presence of an anticlockwise hysteretic behavior, and the reduction of the drain current level suggest a re-adsorption of oxygen molecules by the nanoparticulated film. Therefore, a second UV irradiation step combined with wet-air can be performed. After a second treatment, it is possible to observe a recovery of the aging effects (Figure 4.55). As previously discussed, this treatment is stable over long periods of time even considering a transistor without the application of a passivation layer and integrated using nanoparticles that did not undergo any sintering step. The transfer and output characteristics of the TFT analyzed again two months later are depicted in Figure 4.56. Despite the slight hysteretic behavior displayed in the transfer characteristic and a minor degradation of

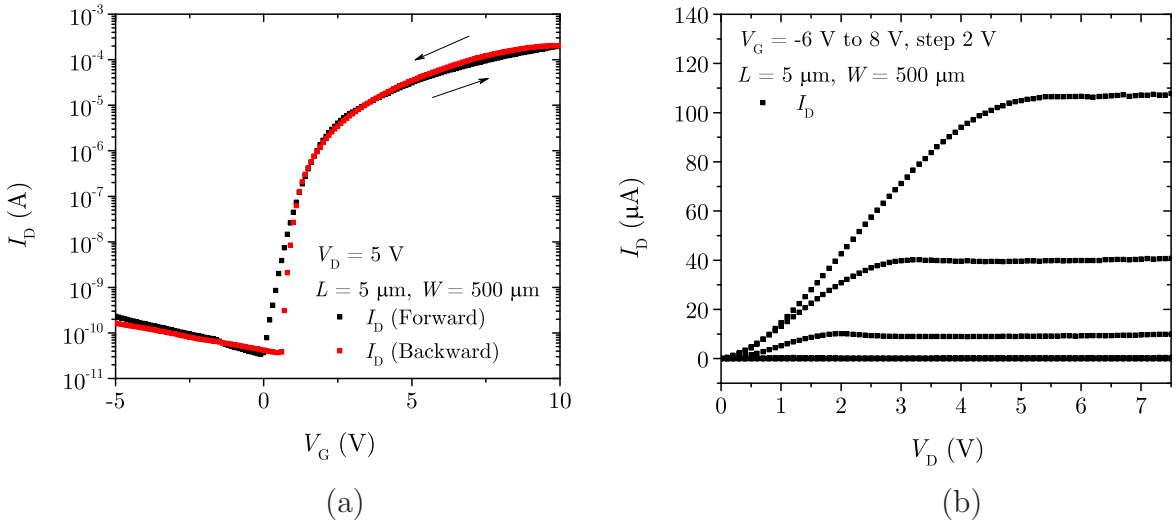


Figure 4.55: Transfer (a) and output (b) characteristics of a ZnO nanoparticle TFT on borosilicate glass substrate applying an inverted staggered setup depicting recovery after a second UV and high humidity treatment.

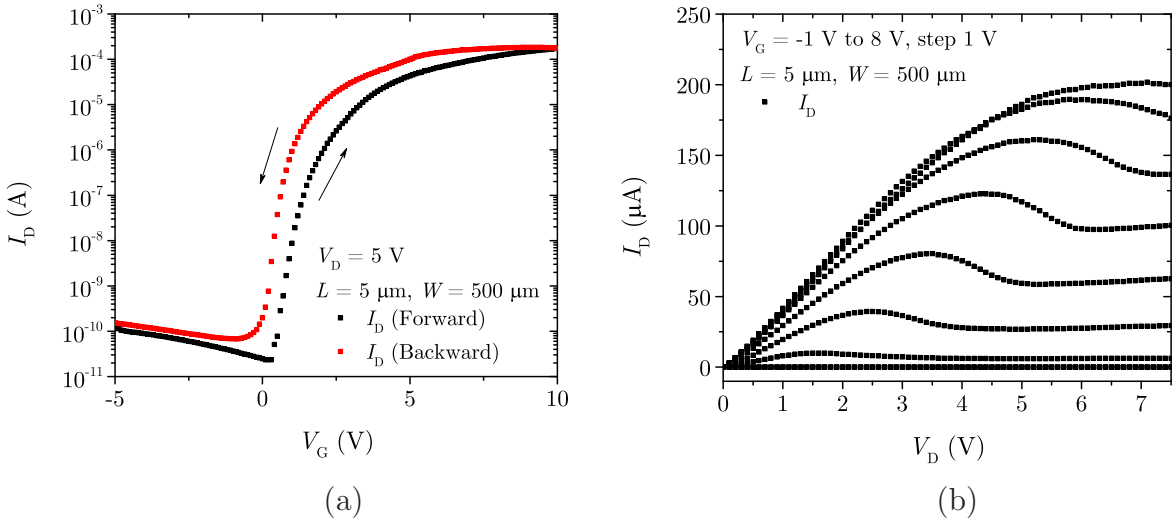


Figure 4.56: Transfer (a) and output (b) characteristics of a ZnO nanoparticle TFT on borosilicate glass substrate applying an inverted staggered setup after two months of storage.

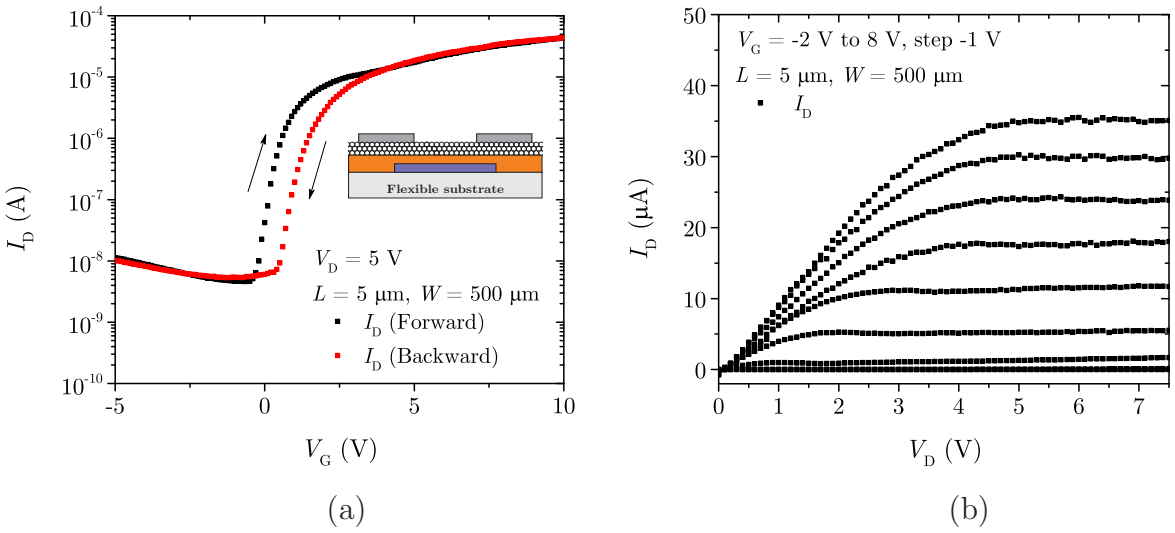


Figure 4.57: Transfer (a) and output (b) characteristics of a ZnO nanoparticle TFT on PET substrate applying an inverted staggered setup. The inset depicts the cross-section of the TFT.

the drain current in the saturation regime, the transistors operate adequately and their metrics have just suffered minor variations

The transfer of the integration process to a flexible substrate holds its main difficulty on the photolithography step upon the nanoparticulated semiconducting film prior to the metal deposition and lift-off technique. On the one hand, overdevelopment of the photoresist may damage the ZnO nanoparticles or cause adhesion issues to the nanoparticulated film. On the other hand, underdevelopment leads to a presence of organic residues below the metallization layer and, therefore, deterioration of the contact quality between the semiconductor and the metal. The transfer and output characteristics of the inverted staggered TFT on freestanding PET substrate is depicted in Figure 4.57. The field-effect mobility (μ_{FE}) is about $0.5\,cm^2V^{-1}s^{-1}$, the subthreshold swing (S) is around 300 mV/dec and the current modulation I_{ON}/I_{OFF} is in the range of 10^4 to 10^5. As expected the turn-on voltage is constant throughout the different transistor setups and the distinct mechanical supports (PET substrate, oxidized Si or borosilicate glass wafer) applied in this study. By comparing the output characteristics of inverted staggered and inverted coplanar setups, an improvement of the contact between the ZnO and the D/S electrodes can be qualitatively observed. However, a decrease in the I_{ON}/I_{OFF} was noticed and ascribed to the increase of the off-state current of the TFT. This leakage current is related to a possible damage of the polymeric matrix of the nanocomposite gate dielectric during the last photolithography step, where an alkaline solution is used as developer. Current

work focuses on the improvement of this step by employing a photoresist which is less aggressive to the dielectric [XOW+15] or by the application of a release layer which is soluble in water [Mic16].

CHAPTER 5

ELECTRONIC CIRCUITS

Aiming at the evaluation of the TFTs in electronic applications, inverters and ring oscillators were also integrated and analyzed. These circuit elements are fundamental to several electronic applications and, thus, their feasibility is the first step towards the integration of complex systems. The integration procedure was described in Chapter 3, whereas the electrical characterization of single transistors was discussed in Chapter 4. The current chapter is divided into two sections: one on inverters, and the other one on ring oscillators. Both electronic circuits were integrated on rigid and flexible substrates.

5.1 Inverters

Since the ZnO nanoparticle TFTs in inverted staggered setup (Section 4.3) depicted an improved performance, inverters were integrated using this structure for evaluation of their characteristics for digital circuit applications. First, the elementary circuits fabricated on rigid substrate (oxidized-Si wafer) are analyzed[29]. Subsequently, the comparison with inverters integrated on PET substrates is presented. The inverters were designed using a load transistor in the pull-up network and an active transistor in the pull-down network. Figure 5.1 shows the schematic circuit and an optical microscope image of an inverter.

[29] The results concerning the inverters using ZnO nanoparticle TFTs on oxidized Si wafer were partially published in [4].

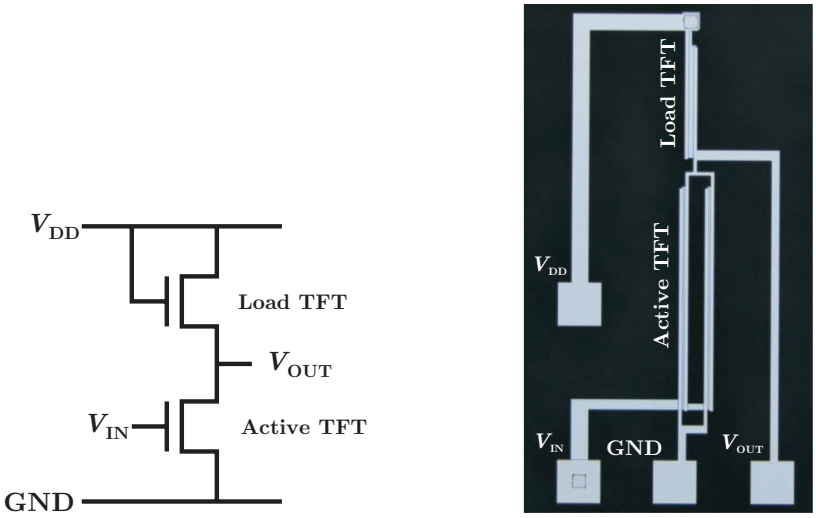


Figure 5.1: Schematic circuit (a) and an optical microscope image (b) of an inverter using ZnO nanoparticle TFTs.

The voltage transfer characteristics (VTC) of a typical inverter at different supply voltages (V_{DD}) are depicted in Figure 5.2. The inverter circuit shows V/V peak gains of approximately 11 for $V_{DD} = 2.5\,V$, and 45 for $V_{DD} = 10\,V$. Additionally, the high and low output voltage levels swing almost the entire supply voltage course, *i.e.* the high output level is comparable to the V_{DD} and the low output level is close to the ground potential, although the inverter uses only a single type of transistor (as load and as active TFTs) instead of a complementary design. Another important aspect is the noise margin (NM) defining the voltage tolerance or the amount of noise that the circuit withstands without compromising its operation. This margin is defined for low levels as $NM_L = V_{IL} - V_{OL}$ and for high levels as $NM_H = V_{OH} - V_{IH}$. The input low voltage (V_{IL}), the output low voltage (V_{OL}), the output high voltage (V_{OH}) as well as the input high voltage (V_{IH}) are extracted from the voltage transfer characteristics at the points where the gain V/V of the inverter is equal to unity. For the inverter characterized in Figure 5.2, the noise margin NM_L is approximately 0.4 V independently of the supply voltage, and the NM_H is about 1 V for $V_{DD} = 2.5\,V$ and around 7.6 V for $V_{DD} = 10\,V$.

The inverter geometry, especially the difference between the load and active transistors' sizes, affects the circuit characteristics, such as the gain and the power consumption. The geometry ratio (β) is defined as the quotient between the W/L relation of the active and the load transistor. Figure 5.3 depicts the average peak gain with different supply voltages and geometry ratios. An increase of this gain is observed when a higher supply

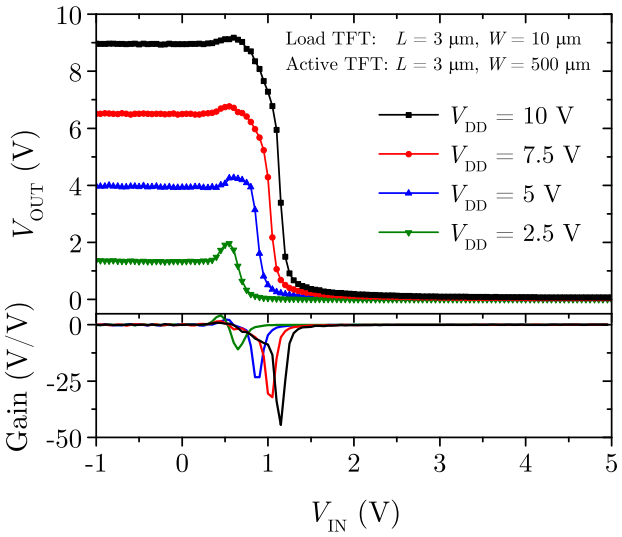


Figure 5.2: Voltage transfer characteristics of a ZnO nanoparticle inverter with different supply voltages. The bottom graph depicts the gain in dependence on the input voltage.

voltage is applied. This effect was noted in all analyzed inverter's geometric ratios but $\beta = 3$. In this case, the active TFT requires a large variation of the input voltage to switch the output voltage level, decreasing the inverter gain. Figure 5.4 shows the peak gain as a function of the inverter geometry. On the one hand, it is possible to recognize an improvement on the gain following the increase in the size difference between the active and the load TFTs. On the other hand, it starts to saturate at $\beta > 25$ indicating that a higher geometry ratio consumes more active area of the substrate without a substantial improvement of the circuit performance and also increasing the production cost.

The hysteretic behavior observed in the $I-V$ curves of the transistors is also transferred to the electrical characteristics of the inverter. An inverter with $\beta = 100$ depicts a difference in the switching point of about 0.6 V when the input voltage (V_{IN}) is swept from logic level 0 to 1 and again vice versa, as shown in Figure 5.5a. This shift in the operation characteristics is proportional to the variation of the V_{ON} observed during the TFT characterization. Circuits with smaller geometry ratios present a lower shift difference (see Figure 5.5b) due to the operating point of the active TFT, which is less sensitive to the hysteretic behavior. However, such inverter requires a higher excursion of the V_{IN} to switch the output level. An approach to improve the switching point and to increase the reliability is the development of a more robust circuit design [HFL+11].

Commonly, inverter circuits applying a single TFT type as load as well as active transistors require more power to operate. Figure 5.6 shows the power consumption as function

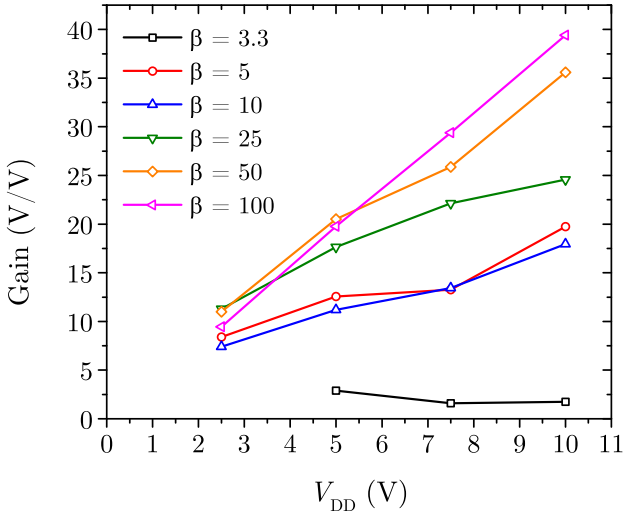


Figure 5.3: Average peak gain of the ZnO nanoparticle inverters in dependence on the supply voltage.

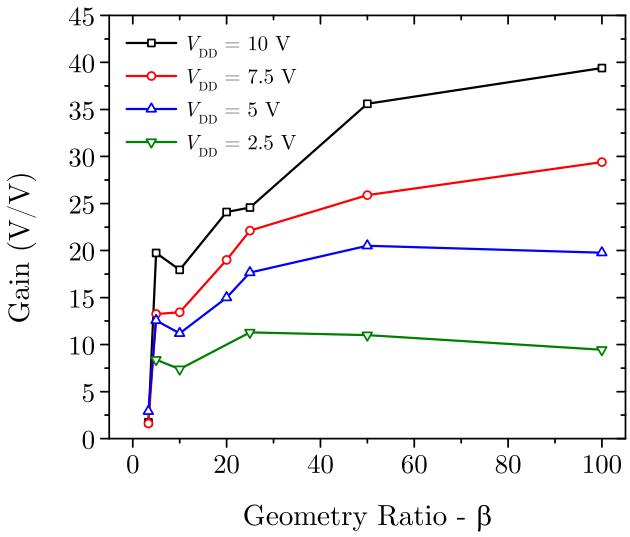


Figure 5.4: Average peak gain of the ZnO nanoparticle inverters in dependence on the geometry ratio.

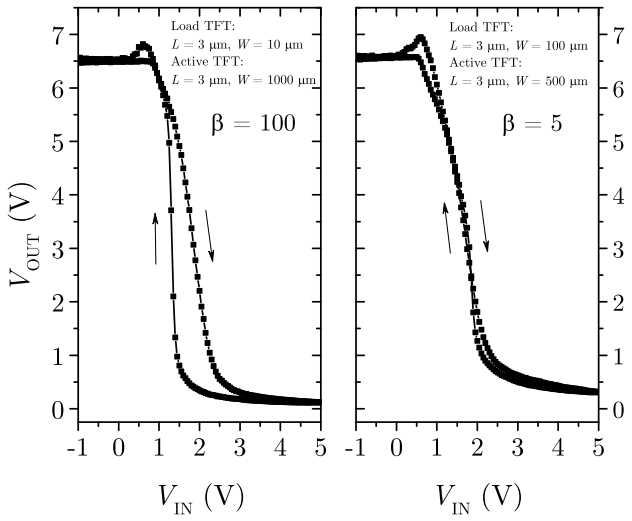


Figure 5.5: Voltage transfer characteristics of a ZnO nanoparticle inverter with geometry ratio (a) equal to 100 and (b) equal to 5 and with $V_{\mathrm{DD}} = 7.5\,\mathrm{V}$.

of the geometry ratio; for inverters with low β, it is higher as the pull-up transistor allows for a relatively high current flow through the circuit. The main consumption occurs when V_{OUT} is at a low-voltage state (V_{IN} is at high state), as both load and active TFTs are conducting. During the high-voltage state of the output, the power consumption decreases to less than $0.1\,\mu\mathrm{W}$ for all geometry ratios as the active transistor is not conducting.

Further improvements regarding the power consumption and the switching characteristics of the inverters can be achieved by a complementary design. Therefore, an organic-based TFT with *p*-type characteristics could be used in the pull-up network instead of a load TFT. First experiments following this approach are presented in Section 6.2. Notwithstanding, the performance of the inverters employing a single transistor type is already adequate for the integration of digital circuits on flexible templates as the integration process is fully compatible to polymeric substrates. Moreover, the inverter metrics are comparable to devices that are integrated using sputtering techniques and high performance materials, or high annealing temperature processes for the semiconducting layer [OAS+07, MSR+14, PMV+16].

In order to evaluate the feasibility to integrate electronic circuits on flexible substrates, inverter circuits were fabricated also on a freestanding PET foil[30], following the process described in Section 3.6.1, firstly applying an inverted coplanar setup. They show V/V

[30] The results concerning the inverters using ZnO nanoparticle TFTs on PET substrates were partially published in [1] and [14].

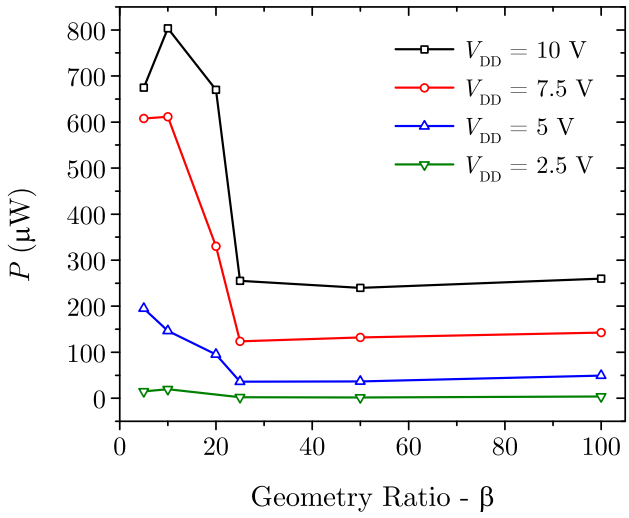


Figure 5.6: Maximum power consumption as a function of the ZnO nanoparticle inverter geometry ratio.

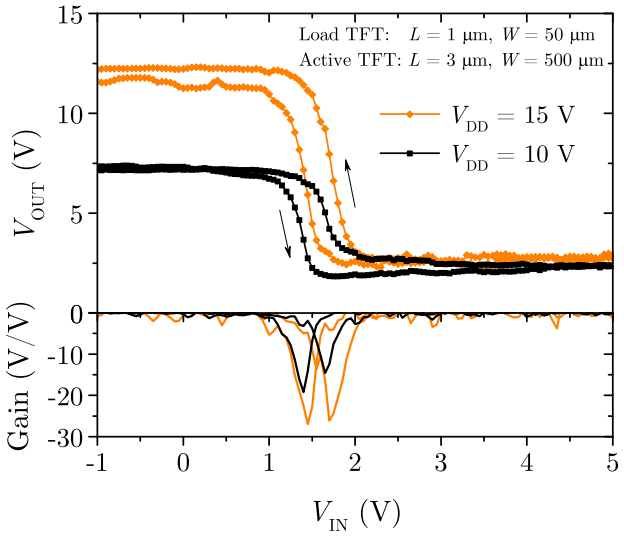


Figure 5.7: Voltage transfer characteristics of an inverter circuit of ZnO nanoparticle devices on PET substrate applying an inverted coplanar setup. The bottom graph depicts the gain in dependence on the input voltage.

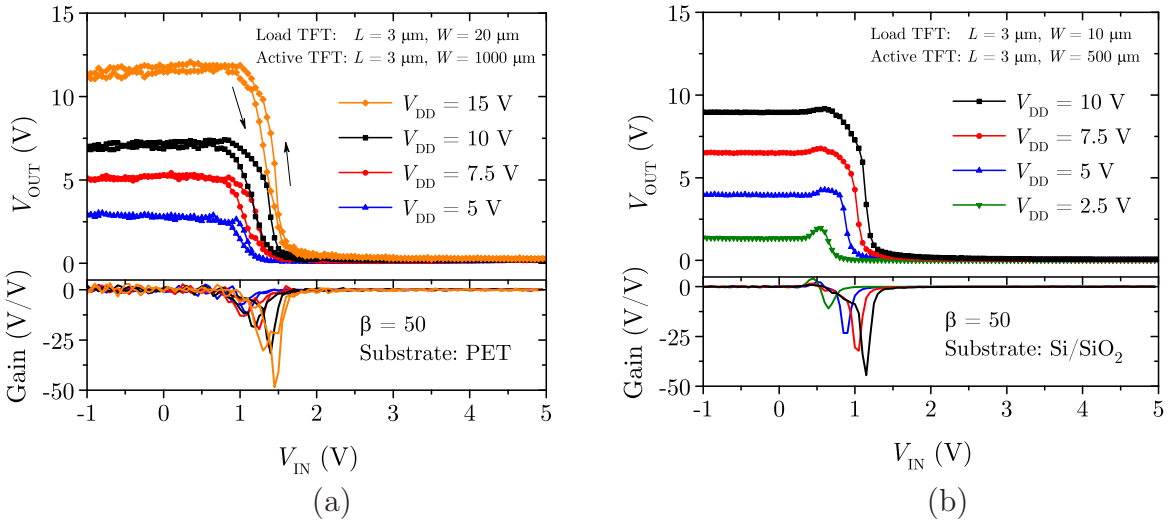


Figure 5.8: Voltage transfer characteristics of a ZnO nanoparticle inverter applying an inverted staggered setup on (a) PET substrate and on (b) oxidized Si wafer with different supply voltages. The bottom graphs depict the gain in dependence on the input voltage.

gain of about 25 for $V_{DD} = 15\,V$ and sufficient performance for electronic circuits. The voltage transfer characteristics is depicted in Figure 5.7.

Inverter circuits were also evaluated applying inverted staggered TFTs on polymeric substrates (Section 4.3), as this type of structures depicts a better performance compared to the employment of inverted coplanar setups. The voltage transfer characteristics of a typical inverter is shown in Figure 5.8a. The V/V peak gain of the devices is about 20 for $V_{DD} = 5\,V$, and around 50 for $V_{DD} = 15\,V$. These inverters have also shown adequate electrical characteristics for the integration of more complex electronic circuits on flexible substrates. Moreover, for comparison reasons, as this study shows successful results of the transfer process from a rigid to a flexible substrate, Figure 5.8b depicts an inverter integrated on an oxidized Si wafer with the same geometry ratio – β. It is possible to note the consistency of the integration process and of the results achieved on both rigid and flexible substrates. Nevertheless, one of the observed differences is related to the higher leakage current for the transistor integrated on the PET substrate (Section 4.3). Due to this aspect, the PET inverter's high voltage levels are lower than the ones on the Si wafer. By selecting a lower geometric ratio, the high-state voltage level can be improved as the load transistor allows for a higher current flow through the circuit. Thus, the leakage current of the active transistor has a reduced effect on the inverter high-level state.

5.2 Ring Oscillators

After the encouraging results obtained from the evaluation of the TFTs on inverter circuits, their dynamic characteristics were also investigated. Therefore, inverters were connected to form a ring oscillator, as shown in Figure 5.9. Two important aspects concerning such circuits should be emphasized: the presence of an output inverter driver (buffer) to avoid major influence of the measurement system on the operation frequency; and the fact that the number of inverters in the ring should be odd, otherwise the circuit will not oscillate.

Ring oscillators are generally utilized to compare the performance of different technologies or circuit styles [RCN03]. Due to the odd number of inverter blocks and the feedback, the circuit operating point is not stable causing the output to oscillate. The oscillation frequency is determined by the propagation time of a signal through the circuit chain. It can be expressed as:

$$f = \frac{1}{T} = \frac{1}{2t_{\mathrm{p}}N} \tag{5.1}$$

where T is the period of the oscillation, t_{p} is the propagation time of each inverter block and N is the number of inverters in the chain of the ring oscillator circuit. The factor 2 is related to the requirement of a full cycle, *i.e.* low-to-high and high-to-low transitions [RCN03].

In this study, ring oscillators employing inverted coplanar setups were first integrated and characterized on rigid substrates (oxidized Si wafer). The output voltage as a function of time is depicted in Figure 5.10. An oscillation of the current can be clearly identified, a strong indication that the integration process is stable enough to fabricate small circuits (> 12 transistors). Nevertheless, a relatively low oscillation frequency is observed; propagation times in the order of $0.3 - 0.5\,\mathrm{s}$ were extracted for a single inverter.

Similar results were achieved when the same integration process was transferred to a polymeric template. Figure 5.11 shows the output voltage of a ring oscillator on a PET substrate over time. In this case, the propagation time of a single inverter is approximately $0.15\,\mathrm{s}$. This outcome (low frequency) can be attributed to these aspects: the low performance of inverted coplanar TFTs in comparison to the inverted-staggered ones, the high-resistive contacts and wiring between the inverter circuits, and the increased fan-in and fan-out caused by parasitic capacitances. Aiming at a higher operation frequency, ring oscillators on rigid substrates (oxidized Si wafer) employing an inverted staggered

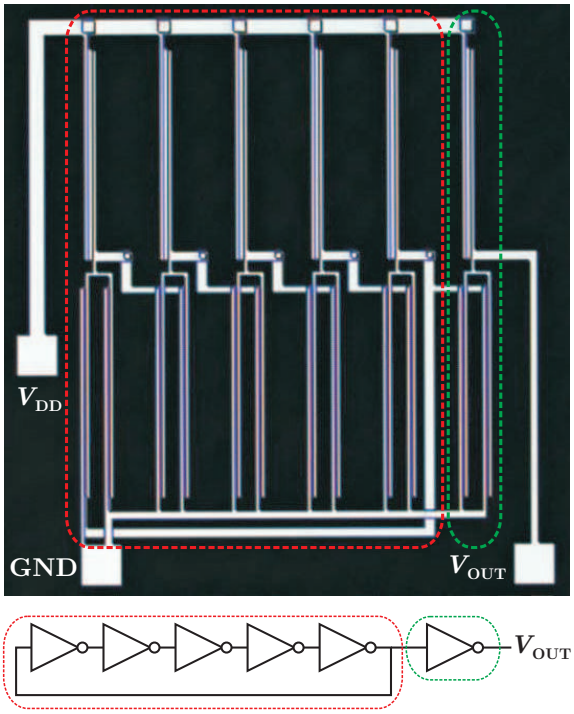


Figure 5.9: An optical microscope image and the schematic circuit of a ring oscillator of 5 stages with an output buffer using ZnO nanoparticle TFTs.

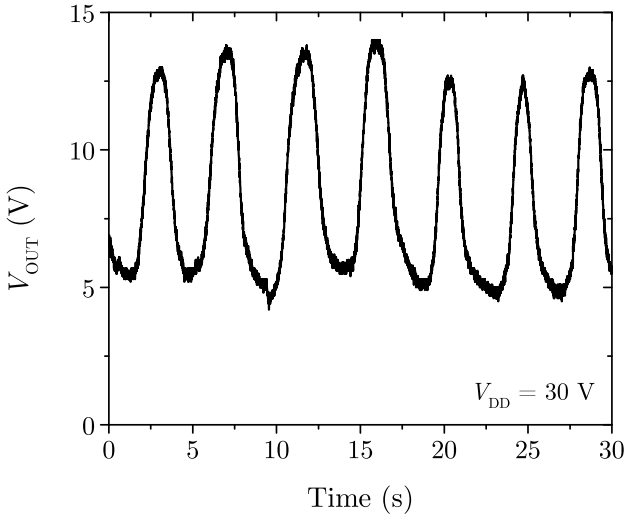


Figure 5.10: Ouput voltage of a ZnO nanoparticle ring oscillator on rigid substrate (oxidized Si wafer) employing inverted coplanar inverters (load TFT: $L = 10\,\mu$m, $W = 250\,\mu$m; active TFT: $L = 1.5\,\mu$m, $W = 1000\,\mu$m). The circuit consists of 5 inverter blocks in the oscillation chain and one output buffer (load TFT: $L = 10\,\mu$m, $W = 250\,\mu$m; active TFT: $L = 1.5\,\mu$m, $W = 1000\,\mu$m).

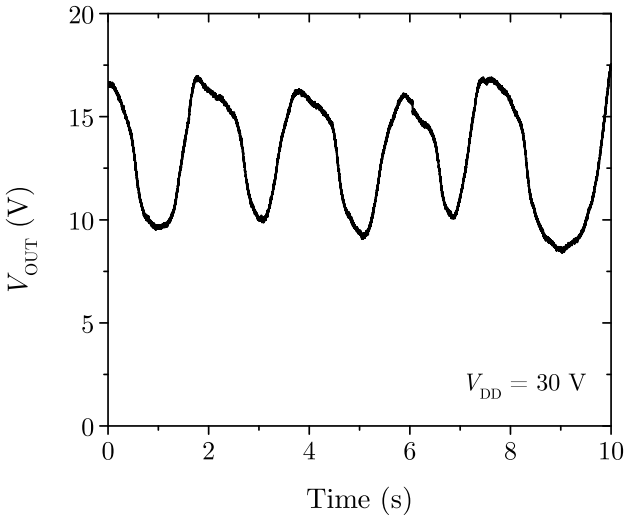


Figure 5.11: Ouput voltage of a ZnO nanoparticle ring oscillator on freestanding PET substrate employing inverted coplanar inverters (load TFT: $L = 10\,\mu$m, $W = 250\,\mu$m; active TFT: $L = 3\,\mu$m, $W = 1000\,\mu$m). The circuits consist of 5 inverter blocks in the oscillation chain and one output buffer (load TFT: $L = 10\,\mu$m, $W = 250\,\mu$m; active TFT: $L = 3\,\mu$m, $W = 1000\,\mu$m).

setup were fabricated. Figure 5.12 depicts the output voltage as a function of the time. By applying this TFT setup, a higher excursion of the output voltage is observed, which is attributed to the improved performance of the transistors as well as of the inverters; however, the oscillation frequency was just slightly affected. Propagation times of around 0.06 s were extracted for a single inverter.

Based on the results achieved applying either inverted coplanar or inverted staggered transistor setups, the main issue regarding the dynamic operation of the TFTs is not related to the performance of each block (transistors), but to the interconnection between them. On the one hand, the employment of a stack of Al and Ti used for the gate electrode has shown advantages regarding the integration of the TFTs on rigid and flexible substrates. On the other hand, the 7-nm thick Ti layer is likely oxidized prior the gate contact opening, leading to a high resistance contact between each inverter block. Another issue is related to the design of the available photolithography mask set, as via connections between each inverter block do not follow a standard design rule; they are smaller than the connections for contacting the electrodes or the ones employed in the inverter circuits. This fact causes instabilities during the fabrication, especially during the development of the photoresist and during the etching processes.

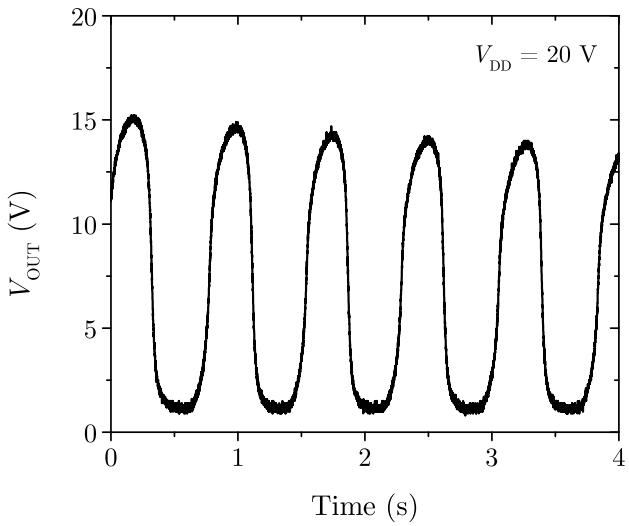


Figure 5.12: Ouput voltage of a ZnO nanoparticle ring oscillator on rigid substrate (oxidized Si wafer) employing inverted staggered inverters (load TFT: $L = 5\,\mu$m, $W = 250\,\mu$m; active TFT: $L = 3\,\mu$m, $W = 1000\,\mu$m). The circuit consists of 5 inverter blocks in the oscillation chain and one output buffer (load TFT: $L = 5\,\mu$m, $W = 250\,\mu$m; active TFT: $L = 3\,\mu$m, $W = 1000\,\mu$m).

Further experiments were performed using silver as the gate electrode material, thus avoiding the highly resistive TiO_2 at the via connections. This material (Ag) was chosen because it depicts adequate selectivity during the etching process of the high-k resin used as the gate dielectric. However, due to etching issues and to local oxidation of the gate electrodes, the deposition quality of the gate insulator was deficient. For this reason, the transistors integrated using this approach displayed low breakdown voltages. The transfer characteristics of an inverted staggered TFT employing Ag as the gate contact material is shown in Figure 5.13.

Ring oscillators were also integrated employing Ag-based contacts as gate electrode. Nonetheless, due to instabilities (oxidation effect) on the gate material, the achievement of a stable operating oscillator was troublesome. Faster circuits were achieved; however, as a result of the gate dielectric breakdown, they oscillated at higher frequencies for a short period, unavailing the collection of the data. Figure 5.14 shows the results of a ring oscillator with Ag-gate contacts. A propagation time of 0.02 s could be extracted for a single inverter circuit due to the presence of a low-performance inverter in the oscillation chain, which enabled the collection of the data before the breakdown. Nevertheless, it is possible to observe sharp edges on the output voltage during the oscillation; this indicates a satisfactory coupling between the oscillating chain and the output inverter driver

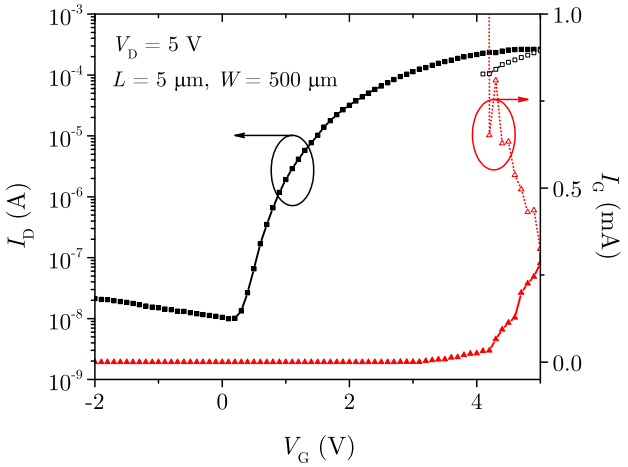


Figure 5.13: Transfer characteristics of a ZnO nanoparticle TFT on rigid substrate (oxidized Si wafer) applying an inverted staggered setup and Ag-based gate electrode. Due to issues (oxidation and defects) on the gate electrode, a dielectric low breakdown voltage as well as high leakage currents were observed. Forward sweep: solid / backward: open.

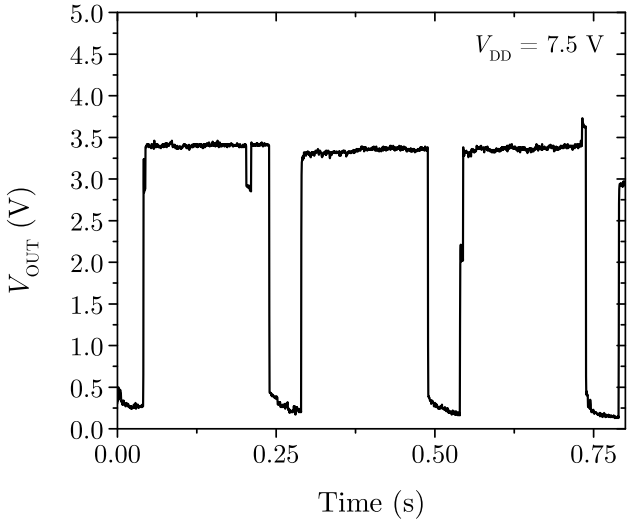


Figure 5.14: Ouput voltage of a ZnO nanoparticle ring oscillator on rigid substrate (oxidized Si wafer) employing inverted staggered inverters (load TFT: $L = 5\,\mu$m, $W = 500\,\mu$m; active TFT: $L = 3\,\mu$m, $W = 1000\,\mu$m) and Ag-based gate contacts. The circuit consists of 5 inverter blocks in the oscillation chain and one output buffer (load TFT: $L = 5\,\mu$m, $W = 500\,\mu$m; active TFT: $L = 3\,\mu$m, $W = 1000\,\mu$m).

(buffer). By considering the edges of the output voltage (rise and fall times), frequencies of around 1 kHz to 1.5 kHz could be estimated in the case of proper via connections. Notwithstanding, considering both, a reliable gate electrode and proper connections between the inverters, much higher frequencies ($>$ MHz) are expected. The wet-etching of the TiO_2 after the opening of the vias exhibited low selectivity to the high-k resin. Further approaches using gold-based electrodes were considered; however, their patterning by lift-off technique resulted in sharp edges, and therefore high gate-leakage currents were reported [Pan06]. Etching of gold is being investigated, although the chemicals needed may damage the PET substrate. Another technique to be evaluated is the employment of a backside photolithographic step using the Al-based gate electrode as a mask and applying a structured protective Au layer, as discussed in-depth in Section 6.1.

CHAPTER 6

IMPROVEMENTS

In this chapter, approaches to improve the TFTs and the electronics circuits presented in this dissertation are evaluated and analyzed. The main aspects considered are the performance enhancement through the reduction of parasitic capacitances and the patterning of the semiconducting layer by a backside exposure photolithographic step. Conjointly, a complementary design for the inverter circuits employing ZnO-based TFTs in the pull-down network and organic-based TFTs in the pull-up network is evaluated. A further improvement related to mass-production compatibility of the integration process was tested: the use of doctor blade technique as a deposition method for the ZnO nanoparticle dispersion.

6.1 Self-Alignment Processes: Reduction of Parasitic Capacitances and Cross-Talk

Parasitic capacitances are one of the limiting aspects in microelectronics, as they are responsible for the reduction of the cut-off frequency and for the increase of power dissipation in circuits [RCN03]. As discussed in Section 5.2, the low frequency depicted by the ring oscillator when employing the TFTs integrated in this study was primary related to the interconnections between inverters and to parasitic capacitances. The latter has its main origin in the capacitive coupling between the wiring and its surroundings, as well as

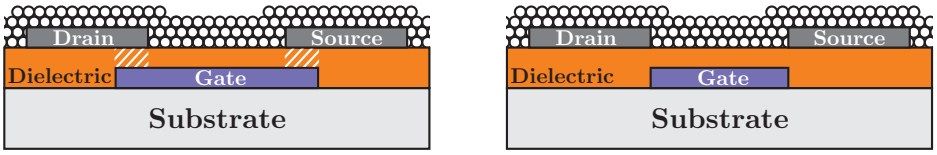


Figure 6.1: Cross-sections of a conventional (a) and a self-aligned (b) TFTs depicting the reduction of the overlapping areas.

in the non-active capacitances of the transistors [RCN03]. Considering the development of the Si-based technology, one of the core issues was the overlapping area between the drain/source and gate electrodes, which was drastically reduced by the implementation of self-alignment processes [Hil14]. Analogously, the reduction of parasitic capacitances can be applied on TFTs by making use of the transparency of the substrate to perform such process[31]. Figure 6.1 allows a comparison between a conventional and a self-aligned transistor.

The fundamentals of this approach were developed in 1964 by Klasens and Koelmans [KK64], who reported a backside exposure process for SnO_2-based transistors. This method reduces the overlapping areas between the drain/source and gate electrodes required for the mask alignment during photolithographic processes. The primary requisite for this technique is that the substrate and gate dielectric materials must be transparent to the exposure lamp irradiation spectra employed in the photolithography. After the structuration of the gate electrodes and dielectric[32] (Figure 6.2a), a positive photoresist is applied and exposed from the backside of the sample through a photomask (Figure 6.2b). Subsequent to the developing process, the drain and source material is deposited (Figure 6.2c) and structured using lift-off technique (Figure 6.2d). Finally, the deposition of the semiconducting material on the sample is performed (Figure 6.2e). Borosilicate glass wafers were primary used for the evaluation of the self-alignment process feasibility. Figure 6.3 depicts the sample with minor overlapping areas between the drain/source and gate electrodes. For the reduction of the overlaps, the exposure time during the photolithography should be adapted; however, effects as light diffraction due to nonhomogeneous

[31] The development of the self-alignment processes for the structuration of TFTs was performed in cooperation with Thorsten Meyers at the Paderborn University. The processes were partially published in [13], [20] and [23].

[32] To simplify, the via connections are not shown in Figure 6.2; however, their structuration can be observed in Figure 3.14 from Section 3.6.1.

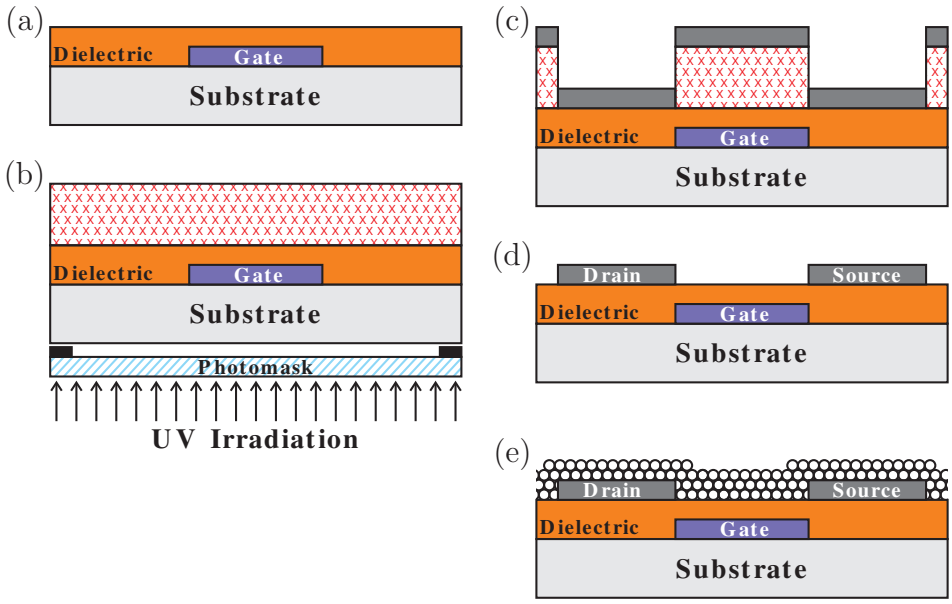


Figure 6.2: Self-alignment process for TFTs employing transparent substrates.

layers, presence of scattering centers caused by the incorporated TiO_2 nanoparticles in the high-k resin, and deposition defects should be considered.

Conjointly, following a similar procedure, the patterning of the semiconducting layer can be arranged in order to reduce cross-talking effects between adjacent TFTs. Therefore, after the integration of the drain and source electrodes (Figure 6.4a), a negative photoresist is applied on the template and exposed from the backside of the sample (Figure 6.4b). The semiconductor material is deposited (Figure 6.4c) and structured by lift-off technique (Figure 6.4d). An optical microscope image of the patterned ZnO layer on a self-aligned TFT is shown in Figure 6.5.

First experiments were focused on the evaluation of the entire self-alignment process for the integration of operating TFTs. Therefore, the transistors were tested after each step of their fabrication. In order to enable the measurement of the TFTs prior to the structuration of the semiconducting layer, the UV irradiation and the high humidity treatment were performed in the presence of the photoresist, despite the possible interference of the organic compound in the ZnO nanoparticles network. Indeed, a slight variation on the V_{ON} was observed and values of approximately 1 V were extracted, as shown in the electrical characteristics of the self-aligned TFT (Figure 6.6). Further instabilities can be related to the larger active area ($W \times L$) of the transistor. Nevertheless, the TFTs present similar characteristics to the previously conventionally integrated devices. A field-effect mobility in the range of $1-2\,cm^2V^{-1}s^{-1}$, I_{ON}/I_{OFF} ratio of about 10^5 and a subthreshold swing of

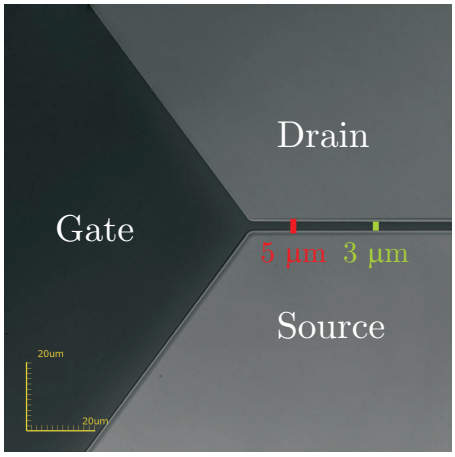


Figure 6.3: Confocal laser microscope image of a self-aligned TFT on a borosilicate glass substrate depicting the transistor's length (green), as well as the transistor's length and overlapping regions (red).

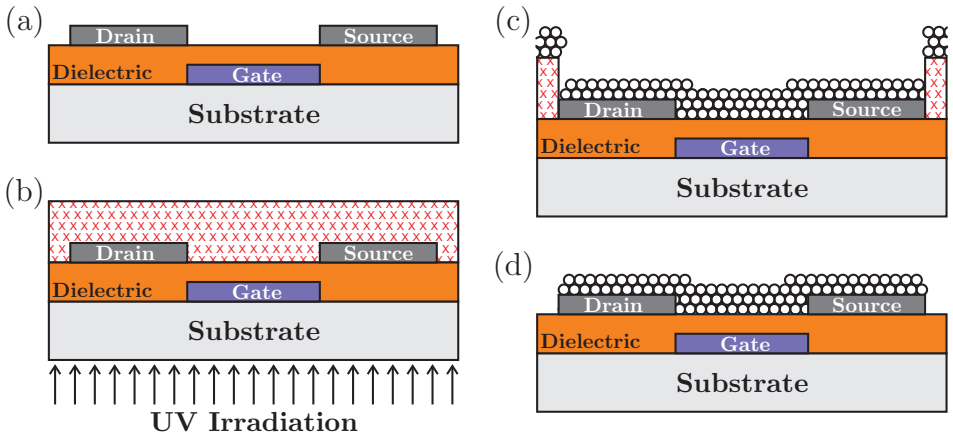


Figure 6.4: Integration process for a self-alignment structuration of the semiconducting layer.

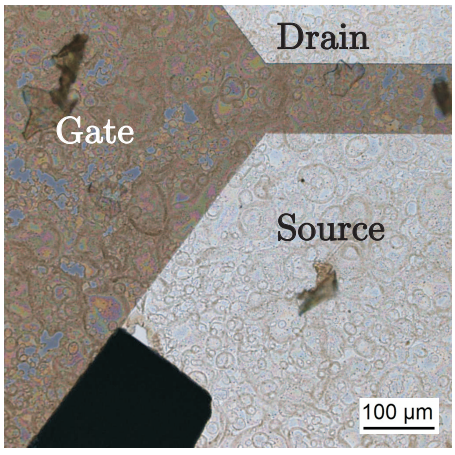


Figure 6.5: Optical microscope image of a patterned ZnO layer on a self-aligned TFT.

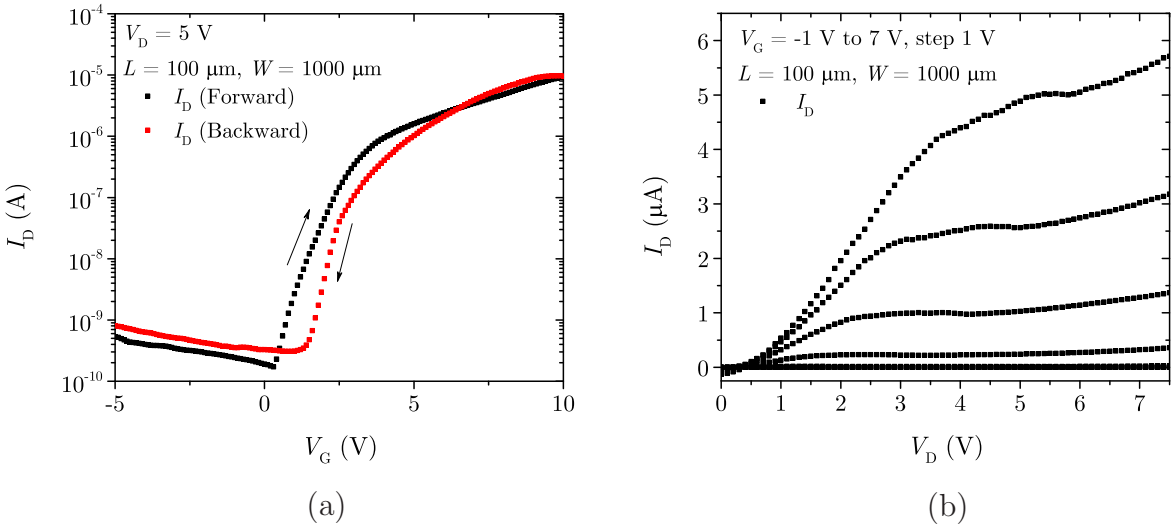


Figure 6.6: Transfer (a) and output (b) characteristics of a self-aligned ZnO nanoparticle TFT on glass substrate.

0.6 V/dec were extracted. After the lift-off process in acetone, the transistors were stored under ambient conditions for 12 h to allow for the vaporization of the solvent from the nanoparticulated layer. Figure 6.7a depicts the transfer characteristics of such transistor; it is possible to observe a strong degradation of the drain current ascribed to the adsorption of O_2 molecules by the ZnO. Therefore, the UV irradiation and the high humidity treatment were repeated; the transfer characteristics are shown in Figure 6.7b. Despite the drain current increase, it did not achieve the same level obtained prior to the lift-off process. Possible reasons are the mechanical stress suffered by the nanoparticles during the ultrasonic bath (lift-off), and acetone contamination on the semiconducting film (the acetone was not washed out, just vaporized at room temperature) prior to the stabilization treatment. Besides the issues encountered during the transistor characterization, the concept of the process is adequate for transparent electronics.

The self-alignment process without the structuration of the semiconducting layer was also evaluated on freestanding flexible substrates. The result, depicted in Figure 6.8, is similar to the ones obtained on the borosilicate glass sample (Figure 6.3). It should be noted, however, that the backside exposure time must be adapted as a function of the higher light absorption of the PET substrate. The transfer and output characteristics of the transistor are shown in Figure 6.9. The turn-on voltage is shifted to lower values ($V_{ON} = 0.5$ V) and the contrast with the values extracted for TFT integrated on the glass sample can be attributed to the absence of the photoresist during the nanoparticle stabilization treatment. Notwithstanding, operating self-aligned transistors were successfully

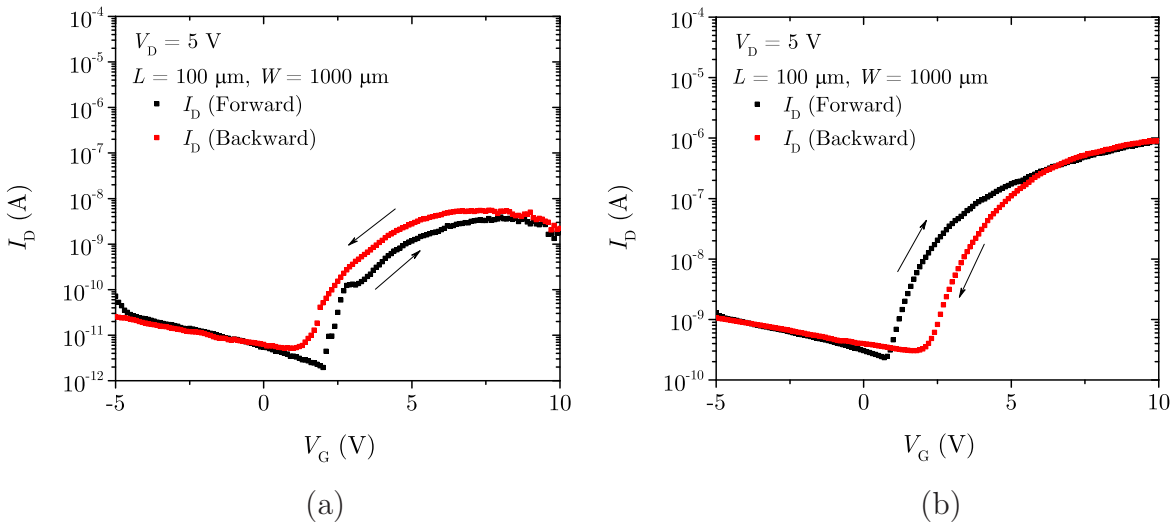


Figure 6.7: Transfer characteristics of the self-aligned ZnO nanoparticle TFT (a) after the semiconducting layer structuration and (b) after the repeat of the UV irradiation and high humidity treatment.

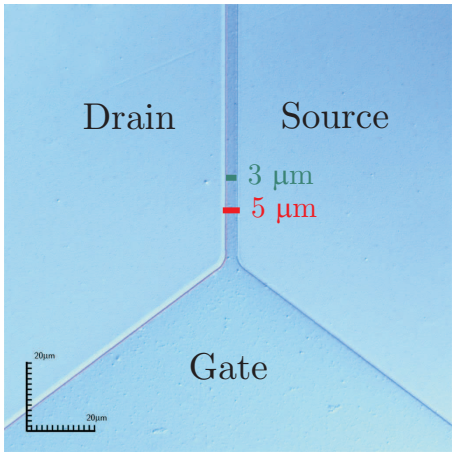
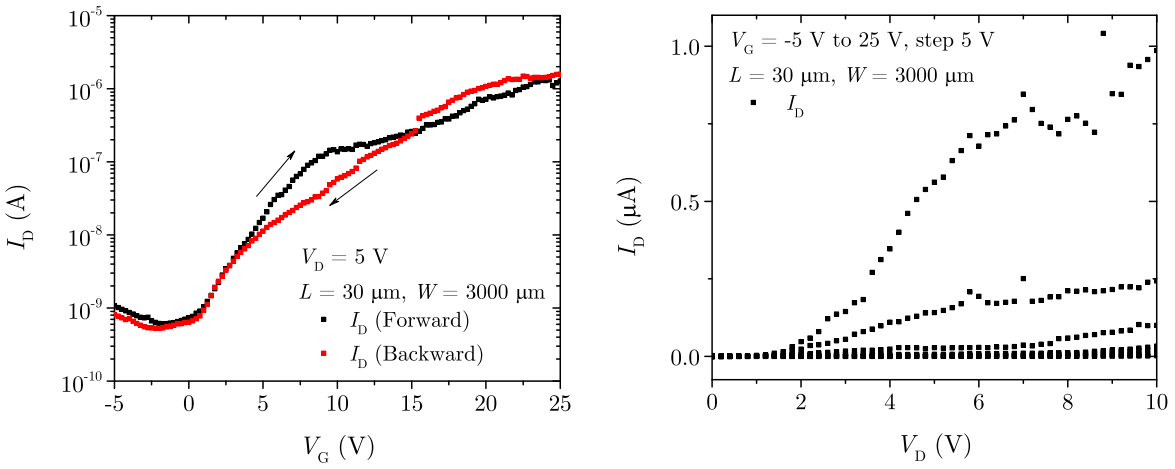


Figure 6.8: Optical microscope image of a self-aligned TFT on a PET substrate depicting the transistor's length (green), as well as the transistor's length and overlapping regions (red).



(a) (b)

Figure 6.9: Transfer (a) and output (b) characteristics of a self-aligned ZnO nanoparticle TFT on freestanding PET substrate.

fabricated on freestanding flexible substrates, indicating the potential of this integration process for transparent and flexible technologies.

Further adaptations to the self-alignment process are under consideration. For the integration of inverted staggered setups, the backside exposure should be performed after the deposition of the active semiconducting layer. Nonetheless, due to the UV-absorption character of the ZnO and to the diffraction effect caused by the nanoparticulated film, the exposure time must also be adjusted. Another improvement to the TFT structuration can be performed by employing similar self-alignment processes to the deposition of an etching-free protective layer for the gate electrodes. Therefore, after their integration, a negative photoresist should be applied and structured by the backside exposure step. In this manner, a thin protective layer (of a few nanometers) with high conductivity and stable to the chemicals used during the via connection opening can be deposited and structured by lift-off technique.

6.2 Complementary TFT Design

Albeit the high performance, the large power consumption of the NMOS technology was one of the reasons for the employment of a complementary design for MOSFETs. This complementary design leads to reduced static power consumption, which is crucial for very-large-scale integration (VLSI) [RCN03]. Such concept can also be applied to the TFT

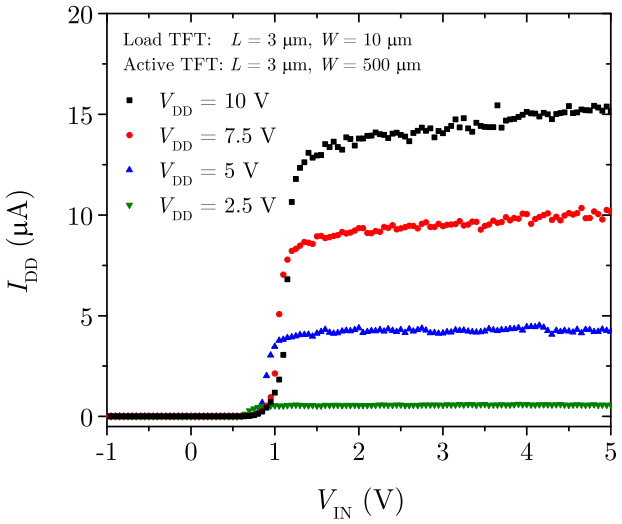


Figure 6.10: ZnO-based inverter circuit current as function of the input voltage.

technology. The TFT-based inverters presented in Section 5.1 were designed applying a load transistor in the pull-up network. Hence, the power consumption when both (active and load) TFTs are conducting is high. Figure 6.10 depicts the current flow through the ZnO-based inverter during the measurement of the voltage transfer characteristics.

In order to optimize the power consumption and to improve the low and high levels of the inverter, a complementary design, using the n-type ZnO-based TFT in the pull-down network and a p-type C_8–BTBT-based TFT in the pull-up network[33], was evaluated. The design difference between a single-type technology and a complementary one is shown in Figure 6.11. Due to the requirements of the organic semiconducting material [Sir14, BL07], the TFTs were integrated using Au as drain and source contacts, even though it causes the leakage current of the inorganic-based transistor to increase [Wol11].

The organic-based TFTs, employing C_8–BTBT, were integrated using the processing described in [2]. The use of the solution-based organic semiconducting material is aligned with the application of the ZnO nanoparticle dispersion; hence, both transistors types are compatible with mass production, as well as with the integration on freestanding flexible substrates. The transfer and output characteristics of a C_8–BTBT-based TFT are depicted in Figure 6.12. The V_{ON} is approximately $-0.7\,V$, I_{ON}/I_{OFF} ratio in the range of 10^4, and μ_{FE} and S are around $0.3\,cm^2V^{-1}s^{-1}$ and $0.5\,V/dec$, respectively. The characteristics related to a ZnO-based TFT with Au drain/source contacts are shown in

[33] The development of the complementary inverter was performed in cooperation with Thorsten Meyers at the Paderborn University. The results were partially published in [17].

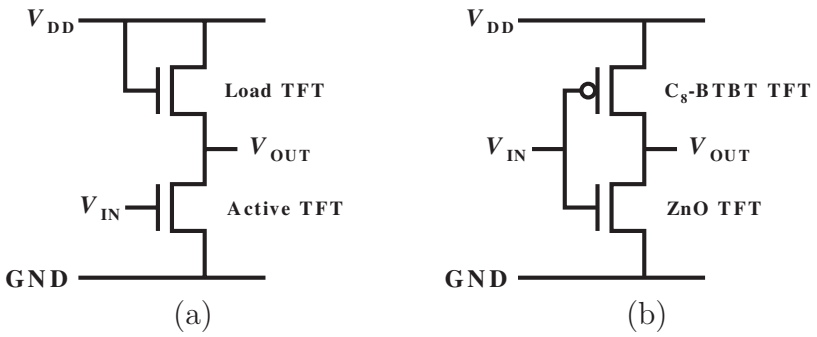


Figure 6.11: Schematic inverter circuit employing (a) a single-type technology and (b) a complementary design.

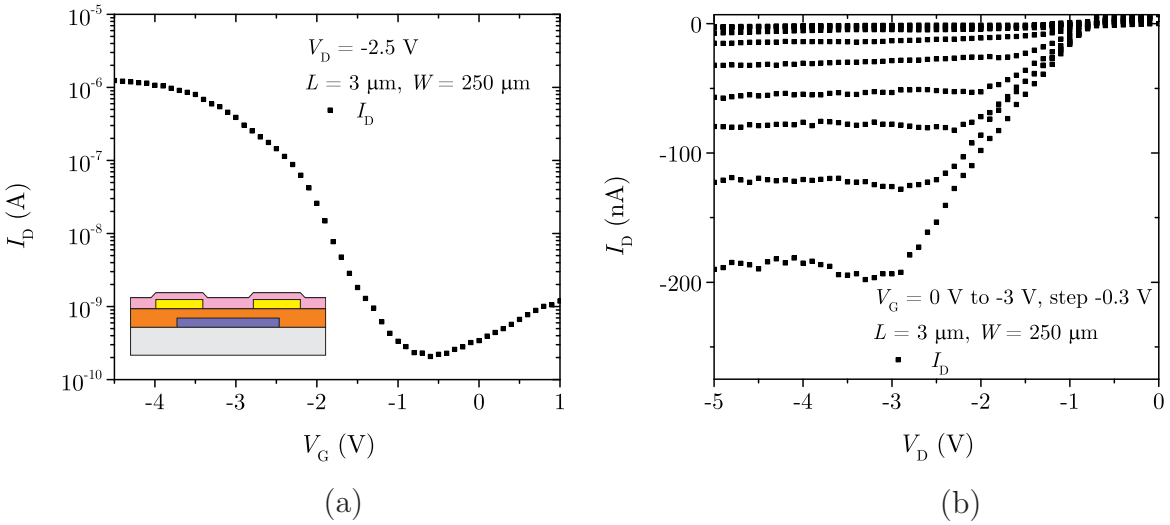
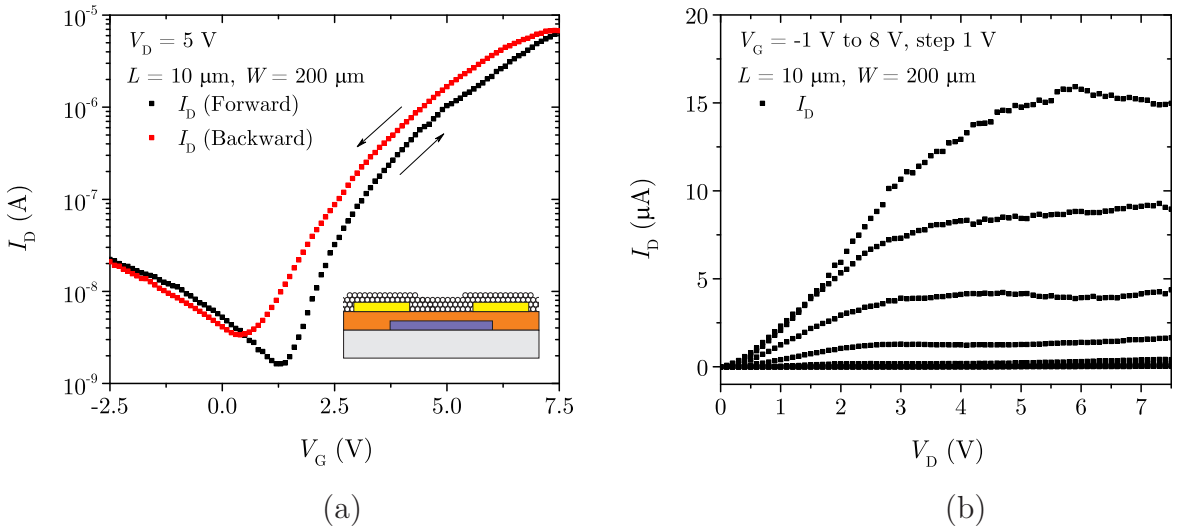


Figure 6.12: Transfer (a) and output (b) characteristics of an inverted coplanar C_8-BTBT-based TFT on a rigid substrate with Au as drain and source electrodes material. The inset depicts the cross-section of the TFT. Measurement data provided by Thorsten Meyers from the Paderborn University – Germany.

Figure 6.13, a V_{ON} of 1 V, I_{ON}/I_{OFF} of around 10^4, μ_{FE} about 0.6 $cm^2V^{-1}s^{-1}$ and S of 1 V/dec were extracted.

By interconnecting both types of TFTs, a complementary circuit is formed, as depicted in Figure 6.11b. The voltage transfer characteristics of the complementary inverter is shown in Figure 6.14. As a consequence of the different current levels, as well as of the relative high leakage current of the ZnO-based TFT in the off-state, the high-level (when V_{IN} is low) of the output voltage is lower than the supply voltage. Nonetheless, a voltage swing of about 80% was achieved in the complementary inverter and peak gains of around 10 were observed. Similar to the ZnO-based inverters presented in Section 5.1,



(a) (b)

Figure 6.13: Transfer (a) and output (b) characteristics of an inverted coplanar ZnO-based TFT on a rigid substrate with Au as drain and source electrodes material. The inset depicts the cross-section of the TFT.

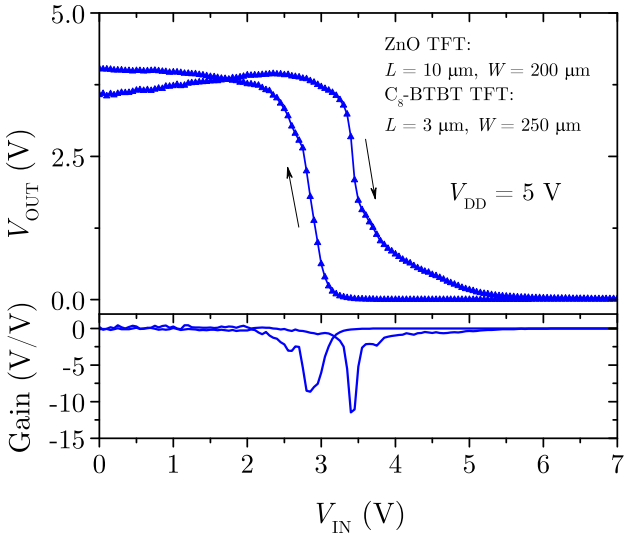


Figure 6.14: Voltage transfer characteristics of a complementary TFT inverter circuit employing ZnO (n-type) and C_8–BTBT (p-type) as semiconducting materials. The bottom graph depicts the gain in dependence on the input voltage.

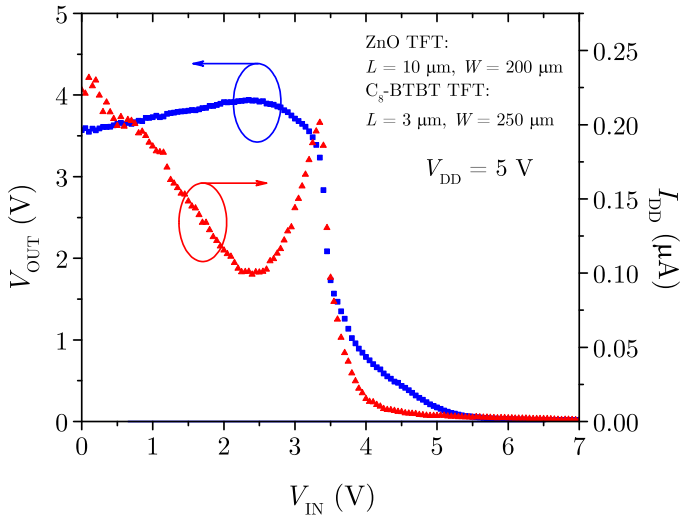


Figure 6.15: Inverter current versus input voltage of the complementary TFT inverter circuit employing ZnO (n-type) and C_8–BTBT (p-type) as semiconducting materials.

this inverter also depicted a slight shift of the operation point depending on the scanning direction of the input voltage.

As expected in the case of complementary design, the current flow through the inverter circuit is reduced in comparison to the single-type technology, as shown in Figure 6.15. However, due to the aforementioned difference in the current levels and to leakage currents, the high level does not reach the supply voltage; this effect also increases the current flow across the circuits at low input voltages. On-going researches from the Sensor Technology Department at the Paderborn University are focused on the performance improvement of complementary circuits employing in(organic)-based TFTs.

6.3 Doctor Blade Deposition

Deposition techniques as roll-to-roll have been employed for centuries by the printed media for mass production of newspapers, for instance. The TFT technology can profit from this know-how, enabling the fabrication of continuous devices on flexible substrates. Among the diverse methods to achieve a layer with homogeneous and controllable thickness, the doctor blade technique is one of the most applied. Aiming at the evaluation of an alternative technique for the deposition of the active semiconducting layer (ZnO nanoparticles),

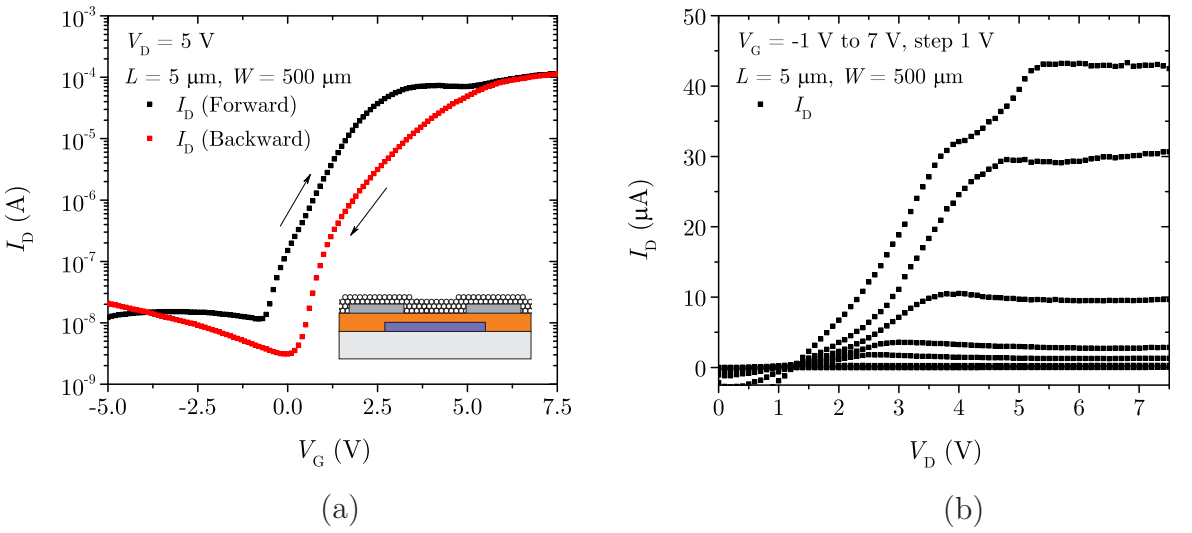


Figure 6.16: Transfer (a) and output (b) characteristics of an inverted coplanar ZnO-based TFT on a rigid substrate employing doctor blade technique for the deposition of the active semiconducting layer. The inset depicts the cross-section of the TFT.

doctor blade was employed on inverted coplanar TFTs with the high-k nanocomposite as gate dielectric and aluminum as drain and source electrodes.

After the integration of the TFT template, the dispersion containing the ZnO nanoparticles was deposited, employing a glass microscope slide as tool to shear the solution onto the sample. The solid content of the dispersion was around 15 wt%, the linear translating speed of the doctor blade was approximately $50\,\mu\mathrm{ms}^{-1}$ and the process was performed under ambient conditions. After the deposition of the active semiconducting layer, the UV irradiation and the high humidity treatment were performed, as described in Section 4.2. The transfer and output characteristics are depicted in Figure 6.16. A V_{ON} of around 0 V, μ_{FE} of about $1.5\,\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$, I_{ON}/I_{OFF} ratio in the range of 10^4 and S of 0.6 V/dec were extracted. It was observed that the transistor characteristics and metrics did not significantly change when either spin- or spray-coating, or doctor blade techniques were used for the deposition of the semiconducting material, despite their inherent differences. This result highlights the robustness of the developed integration process, even applying low-temperature and cost-efficient techniques.

While the doctor blade technique has indeed shown encouraging results, further studies are required to ascertain improvements. The hysteretic behavior in the transfer curve as well as the increased gate leakage current depicted by some transistors indicate that the mechanical stress endured by the template causes instabilities in the TFT opera-

tion. Additionally, because the drain and source electrodes (inverted coplanar setup) are already structured when the doctor blade technique is performed, the direction of the linear translation may influence the orientation of the ZnO nanoparticles (specially for non-spherical shaped nanostructures), hence the performance of the device. Further aspects related to the film, *e.g.* its thickness and the distribution of the nanoparticles, are strongly dependent on parameters such as speed of the process, solid content in the dispersion, evaporation characteristics of the solution, ambient conditions, and surface properties of the template [YJ10, SHK13, DSBM14]. Therefore, a deep investigation of the process is required. Conjointly, in order to avoid the deposition onto already structured electrodes (drain and source), the employment of inverted staggered setups should also be considered.

CHAPTER 7

CONCLUSION AND FUTURE PERSPECTIVES

In this dissertation, the integration process of ZnO-based thin-film transistors on flexible substrates was discussed and analyzed. The techniques employed were strictly selected aiming at a low-cost production and compatibility with flexible substrates. In order to achieve these goals, solution-based processes were primary applied. Therefore, ZnO precursors and dispersions containing ZnO nanoparticles were evaluated as active semiconducting materials. Due to promising characteristics and compatibility with the entire transistor integration process, the investigation was focused on the use of the nanoparticulated ZnO as active semiconducting layer.

ZnO nanoparticle TFTs using poly(4-vynilphenol) (PVP) as gate dielectric were integrated firstly in inverted staggered setups, aiming at an improved performance due to their optimized carrier injection into the semiconducting layer. Nonetheless, a pronounced hysteresis was observed in the TFT transfer characteristics, whereby its value depends on the substrate temperature during characterization. The main causes for this effect were ascribed to dipoles present in the dielectric layer − originated from an incomplete crosslinking reaction of the polymeric dielectric − and to traps located at the semiconductor interface. These two instability mechanisms depict different temperature dependences and lead to the observed change in the hysteretic behavior as a function of the temperature. In order to isolate the main mechanisms responsible for the transistor instabilities, the PVP gate dielectric was replaced by a high-k resin filled with TiO_2 nanoparticles. Using this material, the hysteretic behavior in the transfer characteristics of the TFTs

is significantly reduced. Moreover, due to its higher permittivity, an improved capacitive coupling was observed, lowering the operating voltage of the device. Nonetheless, degradation over time was noted in these transistors. This aging effect was attributed to the high defect density at the nanoparticle surface either related to the large surface area of nanocompounds − which allows for a significant interaction between the semiconductor and the ambient air − or to the chemical stress caused by the processing of the vias and of the drain/source electrodes. For this reason, an inverted coplanar setup was applied. In this way, the semiconductor material deposition is the last step for the integration of the transistor; hence it does not suffer from any chemical and physical stress during further integration processes. Conjointly, taking advantage of this setup, diverse dispersions containing ZnO nanostructures were evaluated as active semiconductor. Moreover, by photoluminescence spectrum analysis, they were characterized; a difference in the deep level emission was observed, which is generally attributed to the defect density in ZnO compounds. Thus, the nanoparticle dispersion with a low defect density and adequate dispersion properties (low agglomeration and sedimentation over time) was selected as the active semiconducting material.

Metal-oxide compounds are known for interacting with the ambient air; this interaction should be avoided when using such compounds as active materials in circuit elements, as device instability may occur. The elements primarily responsible for the variation in the charge carrier concentration in ZnO nanostructures are oxygen and water molecules, which are adsorbed and desorbed from the nanoparticle surface reducing the film conductivity. Oxygen is reported to capture free charge carriers from ZnO depleting its surface, while water molecules desorb the trapped oxygen increasing the charge carrier concentration in the material and improving its conductivity. This effect, however, saturates, as observed during the electrical characterization of the integrated TFT. By employing an UV-irradiation step to assist the desorption of oxygen prior to a high-humidity storage condition, which causes the stabilization of the nanoparticulated film, minor degradation over time was observed.

After the main instability mechanisms in the ZnO nanoparticles TFTs were identified and minimized, which was performed on rigid templates and without a substantial increase of production costs, the transferring of the integration process to freestanding polymeric substrates was initiated. After the successful integration of TFTs on freestanding PET templates employing multiple photomasks and structuration of multiple layers with satisfactory resolution (around 1 μm), the transistor performance was improved by

applying inverted staggered structures. This setup provides a better contact quality between the drain and source electrodes and the active semiconductor. This improvement is attributed to the integration order of the electrodes. As the drain and source material is deposited on top of the semiconducting film, the electrodes follow the roughness and imperfections of the nanoparticulated film increasing the effective contact area. The results, *i.e.* transistors' metrics, achieved using this setup on rigid and on PET substrates are among the best reported for nanoparticle-based TFTs, even though the devices were fabricated applying only low-temperatures and cost-efficient processes compatible with mass production and flexible electronics. Moreover, they are comparable to transistors integrated by high-cost processes or using expensive metal-oxides compounds as well as high temperature annealing steps.

Random telegraph signals (RTS) were observed in the ZnO nanoparticle TFTs. The current level fluctuations were ascribed to active traps located at current paths formed by the nanoparticle network. Depending on the trap state − occupied or empty − the current level shifts to a lower or a higher state, respectively. Furthermore, when multiple traps are active, it is possible to discern different current levels and each one can be associated to a particular active trap. The study of trap activity in nanoparticulated films is an attractive way to investigate reliability aspects of these cost-efficient transistors.

Subsequent to the analyses of the transistors, their application in electronic circuits was evaluated. Therefore, inverter circuits employing a load-transistor in the pull-up network and an active-transistor in the pull-down network were fabricated. The performance of such inverters was analyzed considering the influence of the TFT setup as well as of the substrate used (rigid or flexible). The inverters were characterized evaluating the dependence on the inverter geometric ratio and the supply voltage. They have depicted high V/V gains and adequate switching point characteristics. Further evaluations were focused on the dynamic behavior of such circuits; therefore, ring oscillators were fabricated. Although the encouraging electrical performance exhibited by the ZnO-based inverters, the frequency of the ring oscillators are relative low. This outcome was mainly ascribed to the high resistive contact between the inverters, thus approaches to improve the coupling between circuit blocks were proposed.

Finally, improvements regarding circuit design as well as the integration process were addressed. By an adaptation of the photolithography, a self-alignment process was discussed in order to reduce drastically the overlapping areas between the gate and the

drain/source electrodes, which decreases parasitic capacitances in the circuit. Conjointly, by the employment of a similar process, the cross-talk effect can be minimized through the patterning of the semiconducting layer. Additionally, a complementary design for the TFT technology was also proposed; due to the issues regarding the achievement of soluble low-cost *p*-type metal oxides, organic-based TFTs were combined to the ZnO-based TFTs for the characterization of a complementary technology. Moreover, in order to evaluate another cost-efficient mass-production method, the doctor blade technique was evaluated for the deposition of the active semiconductor.

Summing up, the main goal of this dissertation was achieved; thin-film transistors and electronic circuits were integrated on flexible and transparent substrates using low-temperature and cost-efficient processes. The fabricated devices depict encouraging electrical characteristics; thus, they are suitable for more complex electronic systems. Nevertheless, the path for the development of products using this technology is long and arduous; however, it inspires ambition and fascination. Therefore, in the upcoming section, some approaches and requisites are addressed for future researches.

7.1 Future Perspectives

Flexible and transparent electronic products are already available in the market; this study has given insights on cost-efficient devices on polymeric substrates to be implemented in this technology. The following discussion is focused on some future perspectives, especially regarding the TFTs developed here; nonetheless, some aspects of the entire technology are also addressed.

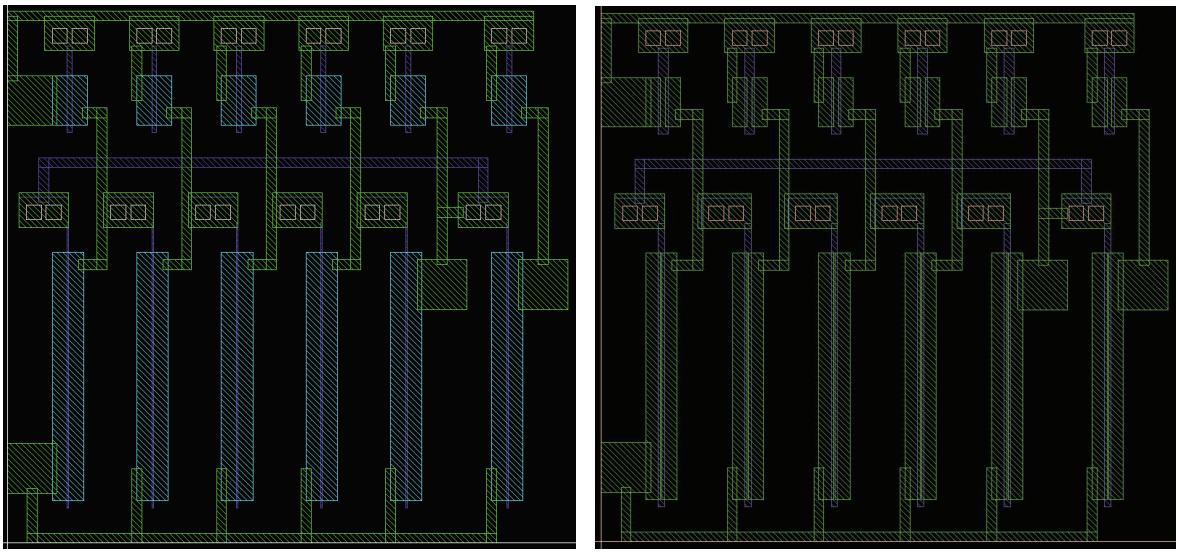
Even though the chosen materials and processes are essential for the achievement of the TFT integration for flexible electronics, bending tests are also required to evaluate the effects of the mechanical deformation on the device's performance. To determine the influence of compressive or tensile strain on the electrical properties of TFTs, a systematic change of the bending radius during the electrical characterization has to be performed. Since the active semiconductor film is formed by nanoparticles, it is expected that the mechanical deformation caused by bending will be released through the nanoparticle network [JPCK09], whereby the main transistor's characteristics will not be significantly affected. In general, compressive and tensile strain cause reversible variations in the channel conductivity until a critical bending radius is reached. After this point, the device

is damaged, originating cracks in the dielectric layer and delamination of the electrodes [SKI+05, SNJ+10]. An enhancement of the flexibility property can be achieved by either reducing the substrate thickness or encapsulating the TFTs in a sandwich construction between a sealant and the substrate [SKI+05]. Recently, Sekitani *et al.* presented a low-voltage organic transistor fabricated on a 12.5 μm thick polymeric substrate covered with an encapsulation stack. The device operated without degradation even at a bending radius of 100 μm [SZKS10]. In addition, the gate dielectric influences the device performance, as the induced strain modifies the capacitances of the dielectric due to changes in the layers thickness (Poisson-effect) and permittivity.

Further investigations concerning the electrical characteristics of the ZnO-based transistors should be carried out. Therefore, statistical analyses of the TFTs are required for a mathematical modeling. The model should cover most of the transistor non-ideality effects, such as the behavior of the metal-semiconductor contacts at the drain and source electrodes, the conduction based on percolation paths, the effects of trap activity, the device variability and the influence of the ambient air. Conjointly, the dynamic characterization of the TFTs and inverters using ring oscillator circuits is also a concern. In order to enhance the contact between the circuit blocks, the via connections must be improved. This can be achieved, for instance, by employing gold-based gate contacts or by depositing a conductive protection layer on top of the electrodes.

Moreover, the influence of the parasitic capacitances on the electronic circuits should also be the focus of future researches. Self-alignment systems, which mitigate such effects, should be further evaluated. In the Sensor Technology Department of the Paderborn University, a new photomask set is being developed in a way to avail the evaluation of the benefits of self-alignment processes to the electrical performance of the devices, as well as a direct comparison between such devices and conventional ones in a single sample. Figure 7.1 depicts an example of the designed structures, in which a ring oscillator with 5 inverters stages and an output driver is shown. Additionally to the comparison of self-aligned and conventional circuits, the fabrication of a complementary technology is also covered in the new photomask design; it is currently being researched in the department.

As briefly discussed, the doctor blade technique depicts encouraging results concerning its employment in a later mass-production fabrication. An in-deep investigation and analysis of its parameters for the deposition of solutions is required. Additionally, depending on the material chosen for the electrodes, *e.g.* a gold nanoparticles dispersion [WLO+05],



(a) (b)

Figure 7.1: Example of ring oscillator designs for the direct comparison of (a) self-aligned and (b) conventional circuits. The design was developed in Virtuoso® Layout Suite XL from Cadence®.

the integration of a fully solution-based device is possible. Aligned with the doctor blade technique, fully printed devices should also be considered, although resolution and device performance reductions are expected. Nevertheless, inkjet technology with subfemtoliter accuracy has also shown some promising characteristics [SNZ+08].

Improvements addressing the transistor transparency may also be taken in account. Therefore, the employment of, for instance, ITO or aluminum doped ZnO as electrodes materials could be evaluated. The current density on these materials as well as adaptations on the self-alignment process should be analyzed. Another approach is the application of a pulsed-laser technique on a single layer of ZnO nanoparticles for the drain and source areas formation [PMK+09, LPK+12]; the D/S electrodes would be these annealed high conductive ZnO regions of the layer, hence transparent. Nevertheless, damage to the gate dielectric and an increase of the leakage currents may occur.

Considering the semiconducting layer, along with the analyses of the trap activity in the film, the improvement of nanoparticle connections and the reduction of their defect density are also required. The employment of acetate-based ZnO precursor on the nanoparticulated ZnO has shown some interesting results; however, due to the applied low temperatures, a partial decomposition of the Zn salt was observed. The use of a mixture of the ZnO nanoparticle dispersion with the nitrate-based precursor should be

investigated, as this compound requires a lower synthesis temperature. Nonetheless, the sensitivity of the high-k nanocomposite applied as gate dielectric may impose limitations. Also, the development and application of a passivation layer to increase the life-time of the devices is necessary, although it may increase the fabrication costs.

For the structuration of the transistors and electronic circuits presented in this study, conventional contact lithography was used; however, this technique is not suitable to continuous substrates. The application of a photolithographic system directly employed in a roll-to-roll process [LLPK16] is expected to solve such limitation and to enable the fabrication of the devices on a continuous substrate for mass production.

After the addressing of the aforementioned aspects, more complex electronic circuits, such as NAND, NOR and XOR digital gates, should be implemented in either single type or complementary technology employing self-aligned and conventional structures. Additionally, the evaluation of an arithmetic logic unit (ALU) should be one of the priorities subsequent to the evaluation of simple combinational circuits.

In the middle of 2016, an interesting roadmap [LRV+16] considering the main aspects and issues of oxide electronic materials and interfaces was published by a cooperation of several research groups around the world. Aspects regarding the employment of metal-oxide compounds in nanoscale form and their composition were addressed, and insights on the requirements and issues of this promising technology were given in diverse fields of application. This confirms the relevancy of this study as well as of its continuance. Conjointly, the Solid-State Circuit Society from IEEE has published in its 50^{th} anniversary magazine edition [Mas16], the evolution of the microelectronic technology over the last decades, indicating the emergence of hybrid systems to improve not only the device performance but also the user interactivity.

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LIST OF SYMBOLS, ABBREVIATIONS AND ACRONYMS

Symbols

A^{**}	effective Richardson constant
C	capacitance
C_{ins}	gate capacitance per unit area
C_{G}	effective gate capacitance per unit area
C_{sem}	capacitance of the semiconductor per unit area
d_{T}	threshold depth
f	oscillation frequency
e, e^-	electron, elementary charge ($1.602 \cdot 10^{-19}\,\mathrm{C}$)
$\mathscr{E}$	electric field
E_{C}	conduction band
E_{F}	Fermi level
E_{V}	valence band
g_{m}	transistor transconductance
h	thickness of the accumulation layer in the semiconductor
$I_{\mathrm{DS}}, I_{\mathrm{D}}$	drain-source current
$I_{\mathrm{GS}}, I_{\mathrm{G}}$	gate-source current

I_{OFF} ..... transistor off-state current

I_{ON} ..... transistor on-state current

J ..... current density

J_{o} ..... saturation current density

k ..... Boltzmann constant

k ..... relative permittivity

L ..... channel length of the transistor

n ..... charge carrier density

N ..... number of inverters in the chain of the ring oscillator circuit

NM ..... noise margin of inverter circuits

NM_{L} ..... noise margin for low levels

NM_{H} ..... noise margin for high levels

q ..... elementary electric charge ($1.602 \cdot 10^{-19}\,\mathrm{C}$)

Q ..... total electric charge

R_{a} ..... roughness average

R_{C} ..... contact resistance

R_{D} ..... contact resistance at the drain electrode

R_{S} ..... contact resistance at the source electrode

S ..... subthreshold swing

T ..... temperature

T ..... period of the oscillation

t_{p} ..... propagation time

t_{ins} ..... thickness of the insulator

t_{int} ..... position of the semiconductor/gate dielectric interface

t_{sem} ..... thickness of the semiconductor

V ..... applied voltage

V_{DD} ..... supply voltages

$V_{\mathrm{DS}}, V_{\mathrm{D}}$ ..... drain-source voltage

$V_{\mathrm{GS}}, V_{\mathrm{G}}$ ..... gate-source voltage

V_{IH} ..... input high voltage of inverter cicuits

V_{IL} ..... input low voltage of inverter circuits

V_{IN} ..... input voltage

V_{OH} ..... output high voltage of inverter circuits

V_{OL} ..... output low voltage of inverter circuits

V_{ON} ..... turn-on voltage

V_{OUT} ..... output voltage

V_{T} ..... threshold voltage

W ..... channel width of the transistor

β ..... geometry ratio of inverter circuits

$W_{\phi_{\mathrm{Bn}}}$ ..... width of the metal-semiconductor barrier

$\Delta\phi$ ..... image-forced lowering of the barrier height

ϵ_0 ..... vacuum permittivity

ϵ_{ins} ..... relative permittivity of the insulator

ϵ_{s} ..... relative permittivity of the semiconductor

η ..... ideality factor

λ ..... wavelength

μ ..... charge carrier mobility

μ_{avg} ..... average mobility

μ_{eff} ..... effective mobility

μ_{FE} ..... field-effect mobility

μ_{inc} ..... incremental mobility

μ_{sat} ..... saturation mobility

ϕ_{Bn} ..... barrier height on a n-type semiconductor

ϕ_{m} ..... work function of a metal

χ ..... electron affinity

Chemical Elements and Compounds

Ag	silver
Al	aluminum
AlN	aluminum nitride
Al_2O_3	aluminum oxide
Ar	argon
Au	gold
Cd	cadmium
CdS	cadmium sulfide
CH_3-COOH	acetic acid
Cl	chlorine
CH_3F	fluoromethane
Cu	copper
Ga	gallium
GaAs	gallium arsenide
GaZnO	gallium zinc oxide
He	helium
HNO_3	nitric acid
H_2O	water molecule
H_2O_2	hydrogen peroxide
H_3PO_4	phosphoric acid
I	iodine
In	indium
In_2O_3	indium oxide
InGaO	indium gallium oxide
InGaZnO	indium gallium zinc oxide
InZnO	indium zinc oxide

$NaOH$	sodium hydroxide
N_2	nitrogen
NH_4F	ammonium fluoride
NH_4OH	ammonium hydroxide
OH^-	hydroxide
O_2	oxygen
Si	silicon
a-Si	amorphous Si
a-Si:H	hydrogenate amorphous silicon
poly-Si	polycrystalline silicon
SiO	silicon monoxide
SiO_2	silicon dioxide
Sn	tin
SnO_2	tin dioxide
Ti	titanium
TiO_2	titanium dioxide
V_o	oxygen vacancies
Zn	zinc
Zn_i	zinc interstitials
$Zn(Ac)_2$	zinc acetate
$Zn(NO_3)_2$	zinc nitrate
ZnO	zinc oxide
$ZnO \cdot x\,H_2O$	zinc oxide hydrate
$Zn(OH)_2(NH_3)_x$	ammine-hydroxo zinc
ZnSnO	zinc tin oxide

Abbreviations and Acronyms

2-ME	2-methoxyethanol
ALD	atomic layer deposition
ALU	arithmetic logic unit
AMOLED	active-matrix organic light-emitting diode
AZO	aluminum zinc oxide
C_8–BTBT	2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene
CCD	charge-coupled device
CYTOP	poly(perfluorobutenylvinylether)
D	drain electrode
DLE	deep-level emission
DNTT	dinaphtho[2,3-b:2,3-f]thieno[3,2-b]thiophene
FE	field-emitted charge carriers
GIZO	indium gallium zinc oxide
GZO	gallium zinc oxide
HOMO	highest occupied molecular orbital for organic materials
HVPE	hydride or halide vapor-phase epitaxy
IEEE	Institute of Electrical and Electronics Engineers
IGO	indium gallium oxide
IoE	Internet of Everything
IoT	Internet of Things
ITO	indium tin oxide
IZO	indium zinc oxide
LCD	liquid-crystal display
LUMO	lowest unoccupied molecular orbital for organic materials
MBE	molecular-beam epitaxy
MOCVD	metal-organic chemical-vapor deposition

MOSFET ..... metal-oxide-semiconductor field-effect transistor
NBE ..... near-band edge emission
NMP N-methyl-2-pyrrolidone
PC ..... polycarbonate
PDMS ..... polydimethylsiloxane
PECVD ..... plasma-enhanced chemical vapor deposition
PEEK ..... polyether ether ketone
PEN ..... polyethylene naphthalate
PET ..... polyethylene terephthalate
PES ..... polysulfone
PGMEA ..... propylene glycol methyl ether acetate
PI ..... polyimide
PL ..... photoluminescence
PLD ..... pulsed-laser deposition
PMCF-m ..... poly(melamine-co-formaldehyde)-methylated
PMMA ..... poly(methylmethacrylate)
PP ..... polypropylene
PS ..... polystyrene
PTFE ..... poly(tetrafluoroethene)
PVA ..... poly(vinylalcohol), polyvinyl alcohol
PVC ..... polyvinyl chloride
PVP ..... poly(4-vinylphenol)
RF ..... radio-frequency
RFID ..... radio-frequency identification
RH ..... relative humidity
RIE ..... reactive ion etching
RTS ..... random telegraph signal
S ..... source electrode
SRAM ..... static random-access memory

TE	thermionic-emitted charge carriers
TFE	thermionic-field emitted charge carriers
TFT	thin-film transistor
UV	ultraviolet
UV−Vis	ultraviolet-visible
VLSI	very-large-scale integration
VTC	voltage transfer characteristic
ZTO	zinc tin oxide

PUBLICATIONS

Articles in Scientific Journals

[1] **Vidor, F. F.**; Meyers, T.; Müller, K.; Hilleringmann, U.: Inverter circuits on freestanding flexible substrate using ZnO nanoparticles for cost-efficient electronics. In: *Solid-State Electronics*, *under revision (major)*

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